

## DDR2 SDRAM SODIMM

### Features:

- 200 pin small-outline, dual in-line memory module (SODIMM)
- Fast data transfer rates PC2-4200 and PC2-5300
- Utilizes DDR2-533 and DDR2-667 SDRAM FBGA components.
- 1GB (128MX64)
- Vdd = 1.8V, VddQ = 1.8V
- VDDSPD = 1.7V to 3.6V
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- 64ms, 8,192-cycle refresh
- Programmable burst lengths: 4 or 8
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency – 1 tck
- On-die termination (ODT)
- Serial Presence Detect (SPD) with EEPROM
- Gold edge contacts
- Dual Rank

### Options:

16 - 64Mx8 DDR2 FBGA    PD128M6416U27YS2X-XX  
 PD128M6416U37YS2X-XX

### Part Number:

#### KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	CAS Latency
-37E	-37E	266MHZ	4
-3	-3	333MHZ	5

### GENERAL DESCRIPTION

The PD128M6416(XXX)S2J is high performance dynamic random-access 1GB module respectively. These modules are organized in a x64 configuration, and utilize quad bank architecture with a synchronous DDR2 interface. These DDR2 SDRAM SODIMM modules use double data rate architecture to achieve high speed operation.

### ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss.....-1 to 2.3V  
 Voltage on VddQ Supply relative to Vss.....-0.5V to 2.3V  
 Voltage on Vref and Inputs relative to Vss.....-0.5V to 2.3V  
 Voltage on I/O pins relative to Vss... -0.5V to VddQ +0.5V  
 Operating Temperature T<sub>A</sub> (Ambient) ..... 0 ° to 85 °C  
 Storage Temperature.....-55 to +100 °

Stresses beyond these may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect reliability.

### PIN ASSIGNMENT

#### 200-Pin DDR2 SODIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vref	51	DQS2	101	A1	151	DQ42
2	Vss	52	DM2	102	A0	152	DQ46
3	VSS	53	Vss	103	VDD	153	DQ43
4	DQ4	54	Vss	104	VDD	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	VSS
6	DQ5	56	DQ22	106	BA1	156	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48
8	Vss	58	DQ23	108	RAS#	158	DQ52
9	Vss	59	Vss	109	WE#	159	DQ49
10	DM0	60	Vss	110	S0#	160	DQ53
11	DQS0#	61	DQ24	111	VDD	161	VSS
12	Vss	62	DQ28	112	VDD	162	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	CK1
15	VSS	65	Vss	115	S1#	165	VSS
16	DQ7	66	Vss	116	NC	166	CK1#
17	DQ2	67	DM3	117	VDD	167	DQ56#
18	Vss	68	DQS3#	118	VDD	168	VSS
19	DQ3	69	NC	119	ODT1	169	DQ56
20	DQ12	70	DQS3	120	NC	170	DM6
21	Vss	71	Vss	121	VSS	171	VSS
22	DQ13	72	Vss	122	VSS	172	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50
24	Vss	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51
26	DM1	76	DQ31	126	DQ37	176	DQ55
27	VSS	77	Vss	127	VSS	177	VSS
28	VSS	78	Vss	128	VSS	178	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
30	CK0	80	CKE1	130	DM4	180	DQ60
31	DQS1	81	VDD	131	DQS4	181	DQ57
32	CK0#	82	VDD	132	VSS	182	DQ61
33	Vss	83	NC	133	VSS	183	VSS
34	Vss	84	NC	134	DQ38	184	VSS
35	DQ10	85	NC/BA2	135	DQ34	185	DM7
36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	VDD	137	DQ35	187	VSS
38	DQ15	88	VDD	138	VSS	188	DQS7
39	VSS	89	A12	139	VSS	189	DQ58
40	VSS	90	A11	140	DQ44	190	VSS
41	Vss	91	A9	141	DQ40	191	DQ59
42	Vss	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	VSS
44	DQ20	94	A6	144	VSS	194	DQ63
45	DQ17	95	VDD	145	VSS	195	SDA
46	DQ21	96	VDD	146	DQS5#	196	VSS
47	Vss	97	A5	147	DM5	197	SCL
48	Vss	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	VSS	199	VDDSPD
50	NC	100	A2	150	VSS	200	SA1

**Spectek Module Part Options and Designations**

<b>Options</b>	<b>Designation</b>
<b>Spectek Module</b>	PD
<b>Module Depth &amp; Width</b> 1GB	128M64
<b>2 Digit chip count</b> 16 chips	16
<b>Design ID</b> Design revision	U27Y U37Y
<b>Module type</b> SODIMM	S
<b>Component type</b> X8	2
<b>Package Type</b> Lead Free FBGA Leaded FBGA	J B
<b>Module Speed Grade</b> DDR2-533 PC2-4200 DDR2-667 PC2-5300	-37E -3

**DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:**

Parameter	Symbol	Min	Nom	Max	Units
Supply Voltage	Vdd	1.7	1.8	1.9	V
VDDL Supply Voltage	VDDL	1.7	1.8	1.9	V
I/O Supply Voltage	VddQ	1.7	1.8	1.9	V
I/O Reference Voltage	Vref	0.49 x VddQ	0.50 x VddQ	0.51 X VddQ	V
I/O Termination Voltage (system)	Vtt	Vref - 0.04		Vref + 0.04	V
Input Leakage Current Any input = 0V ≤ VIN ≤ Vdd All other pins not under test = 0V	Command/Address WE#, RAS#, CAS#, CKE, S#	I <sub>i</sub>	-40	40	uA
	CK0, CK0#	I <sub>i</sub>	-10	10	uA
	CK1, CK1#, CK2, CK2#	I <sub>i</sub>	-15	15	uA
	DM	I <sub>i</sub>	-5	5	uA
Output Leakage Current DQs are disabled; 0V ≤ VOOUT ≤ VddQ	I <sub>oz</sub>	-5		5	uA
Vref Leakage Current; Vref = Valid Vref level	Ivref	-16		16	uA

**AC INPUT OPERATING CONDITIONS:** (This parameter is sampled. Vdd = +1.8V ± 0.1V, VddQ = +1.8V ±0.1V)

Parameter	Symbol	MIN	MAX	Units
Input High (Logic 1) Voltage	VIH (AC)	Vref +0.250		V
Input Low (Logic 0) Voltage (-37E)	VIL (AC)		Vref +0..250	V
Input Low (Logic 0) Voltage (-3)	VIL (AC)		Vref +0..200	V

**DC INPUT OPERATING CONDITIONS:** (This parameter is sampled. Vdd = +1.8V ± 0.1V, VddQ = +1.8V ±0.1V)

Parameter	Symbol	MIN	MAX	Units
Input High (Logic 1) Voltage	VIH (DC)	Vref +0.125	VddQ + .300	V
Input Low (Logic 0) Voltage	VIL (DC)	-.300	Vref +0..125	V

**IDD OPERATING CONDITIONS AND MAXIMUM LIMITS:** Vdd = 1.8V ± .1V, Temp. = 0° to 85 °C

Supply Current	Symbol	-3	-37E	Units
Operating on device bank active-precharge current: Tck=tck(IDD), trc=trc(IDD), tras=tras MIN(idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	Idd0	760	680	mA
Operating one device bank active-read-precharge current: Iout=0mA; BL=4, CL=CL(IDD), AL=0; tck=tck(IDD), trc=trc(IDD), tras=tras MIN(IDD), trcd=trcd(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	Idd1	880	800	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; tck=tck(IDD) CKE is LOW, Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Idd2P	80	80	mA
Precharge quiet standby current: All device banks Idle; Tck = Tck(IDD) CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Idd2Q	800	640	mA
IDLE STANDBY CURRENT: All device banks idle: tck = tck(IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching Data bus inputs are switching	Idd2N	880	720	mA
ACTIVE POWER DOWN STANDBY CURRENT; All device banks open; tck = tck(IDD) CKE is LOW; Other control and address bus inputs are STABLE; Data bus input are FLOATING	Idd3P	560	480	mA
ACTIVE STANDBY CURRENT: All device banks open; tck=tck(IDD), tras=tras MAX(IDD) trp=trp(IDD); CKE is HIGH,S# is HIGH between valid commands; other control and address bus inputs are switching; Data bus inputs are switching.	Idd3N	1,040	880	mA
OPERATING BURST WRITE CURRENT; All device banks open, Continuous burst writes; BL=4, CL=CL(IDD), AL=0; tck=tck(IDD), tras=tras MAX(IDD), trp = trp(IDD); CKE is HIGH, S# is HIGH, S# is HIGH between valid commands; Address bus inputs are switching, Data bus inputs are switching	Idd4W	1,280	1,080	mA
OPERATING BURST READ CURRENT: All device banks open, Continuous burst reads, Iout = 0Ma; BL=4, CL=CL(IDD), AL=0, tck=tck(IDD), tras=tras MAX(IDD), trp=trp(IDD), CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	Idd4R	1,440	1,200	mA
Burst refresh current: tck=tck(IDD): Refresh command at every trfc(IDD) interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	Idd5	3,360	3,200	mA

**Continued:**

**IDD OPERATING CONDITIONS AND MAXIMUM LIMITS:** Vdd = 1.8V ± .1V, Temp. = 0° to 85 °C

Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING data bus inputs are FLOATING.	Idd6	80	80	mA
Operating device bank interleave read current: All device banks interleaving reads, Iout=0mA, BL=4, CL=CL(IDD), AL=trcd (IDD)-1 X tck(IDD); tck=tck(IDD), trc=trc(IDD), trrd=trrd(IDD), trcd =trcd(IDD), CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are switching.	Idd7	2,280	2,120	mA

**NOTES:**

AC ELECTRICAL CHARACTERISTICS: Vdd = 1.8 +/- .1V; Temp. = 0° to 85°C

AC CHARACTERISTICS: CLOCK, DATA and Command/Address			-3		-37E		
PARAMETER		SYM	MIN	MAX	MIN	MAX	UNITS
Clock cycle time	CL=5	tCK	3.0	8.0			ns
	CL=4	tCK	3.75	8.0	3.75	8.0	ns
CK high-level width		tCH	0.48	0.52	0.48	0.52	tCK
CK low-level width		tCL	0.48	0.52	0.48	0.52	tCK
Half clock period		tHP	tCH, tCL		tCH, tCL		ps
Clock Jitter		tJITTER	-125	125	-125	125	ps
DQ output access time from clock		tAC	-450	+450	-500	+500	ps
Data-out high-impedance window from clock		tHZ		tAC max		tAC max	ps
Data out low impedance		tLZ	tAC	tAC	tAC	tAC	ps
DQ and DM input setup time relative to DQS		tDSa	300		350		ps
DQ and DM input hold time relative to DQS		tDHa	300		350		ps
DQ and DM input setup time relative to DQS		tDSb	100		100		ps
DQ and DM input hold time relative to DQS		tDHb	175		225		ps
DQ and DM input pulse width (for each input)		tDIPW	0.35		0.35		tCK
Data hold skew factor		tQHS		340		400	ps
DQ-DQS hold, DQS to first DQ to go nonvalid, per access		tQH	tHP-tQHS		tHP-tQHS		ps
Data valid output window (DVW)		tDVW	tQH-tDQSQ		tQH-tDQSQ		ps
DQS input high pulse width		tDQSH	0.35		0.35		tCK
DQS input pulse width		tDQSL	0.35		0.35		tCK
DQS output access time from clock		tDQSCK	-400	+400	-450	+450	ps
DQS falling edge to CK rising –setup time		tDSS	0.2		0.2		tCK
DQS falling edge from CK rising – hold time		tDSH	0.2		0.2		tCK
DQS-DQ skew, DQS to last DQ valid,per group per access		tDQSQ		240		300	ps
DQS read preamble		tRPRE	0.9	1.1	0.9	1.1	tCK
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	tCK
DQS write preamble setup time		tWPRES	0		0		ps
DQS write preamble		tWPRE	0.35		0.25		tCK
DQS write postamble		tWPST	0.4		0.4		tCK
Write command to first DQS latching transition		tDQSS	WL-0.25	WL +0.25	WL-0.25	WL +0.25	tCK
Address and control input pulse width for each input		tIPW	0.6		0.6		tCK
Address and control input setup time		tISa	400		500		ps
Address and control input hold time		tIHa	400		500		ps
Address and control input setup time		tISb	200		250		ps
Address and control input hold time		tIHb	275		375		ps
CAS# to CAS# command delay		tCCD	2		2		tCK
ACTIVE to ACTIVE (SAME BANK) command		tRC	55		55		ns
ACTIVE bank a to active bank b command		tRRD	7.5		7.5		ns
ACTIVE to READ or WRITE delay		tRCD	15		15		ns
Four Bank Activate period		tFAW	37.5		37.5		ns
ACITVE to PRECHARGE command		tRAS	40		40	70,000	ns
Internal READ to precharge command delay		tRTP	7.5		7.5		ns
Write recovery time		tWR	15		15		ns
Auto precharge write recovery +precharge		tDAL	tWR +tRP		tWR +tRP		ns
Internal WRITE to READ command delay		tWTR	10		7.5		ns
PRECHARGE command period		tRP	15		15		ns
PRECHARGE ALL command period		tRPA	tRP + tCK		tRP + tCK		ns
LOAD MODE command cycle time		tMRD	2		2		tCK

Continued:  
**AC ELECTRICAL CHARACTERISTICS:** Vdd = 1.8 +/- .1V; Temp. = 0° to 85°C

AC CHARACTERISTICS: Refresh and ODT		-3		-37E		UNITS
PARAMETER	SYM	MIN	MAX	MIN	MAX	
CKE low to CK, CK# uncertainty	tDELAY	tIS+ tCK+ tIH		tIS+ tCK+ tIH		ns
Refresh-to ACTIVE or REFRESH command interval	tRFC	105	70,000	105	70,000	ns
Average periodic refresh interval	tREFI	7.8		7.8		us
Exit SELF REFRESH to NON-READ command	tXSNR	tRFC(min) +10		tRFC(min) +10		ns
Exit SELF REFRESH to READ command	tXSRD	200		200		tCK
Exit SELF REFRESH timing reference	tISXR	tIS		tIS		ps
ODT turn-on delay	tAOND	2	2	2	2	tCK
ODT turn-on	tAON	tAC (min)	tAC (max) + 700	tAC (min)	tAC (max) +1000	ps
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC (min)	tAC (max) +600	tAC (min)	tAC (max) + 600	ps
ODT turn-on (power down mode)	tAONPD	tAC (min) + 2,000	tAC (max) + 1,000	tAC (min) + 2,000	tAC (max) + 1,000	ps
ODT turn-off (power down mode)	tAOFPD	tAC (min) + 2,000	tAC (max) + 1,000	tAC (min) + 2,000	tAC (max) + 1,000	ps
ODT to power down entry latency	tANPD	3	3	3	3	tCK
ODT power down exit latency	tAXPD	8		8		tCK
ODT enable from MRS command	tMOD	12		12		ns
Exit active power-down to READ command MR[12] = 0	tXARD	2		2		tCK
Exit active power down to READ command MR[12] = 1	tXARDS	7 - AL		7 - AL		tCK
Exit precharge power down to any non-READ command	tXP	2		2	0	tCK
CKE MIN HIGH/LOW time	tCKE	3		3	3	tCK

**SERIAL PRESENCE-DETECT OPERATION** - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

**SPD CLOCK AND DATA CONVENTIONS** - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

**SPD START CONDITION** - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

**SPD STOP CONDITION** - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

**SPD ACKNOWLEDGE** - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

**SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS** (VCC = +3.3V ± 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units
Supply Voltage	V <sub>DDSPD</sub>	1.7	3.6	V
Input High (Logic 1) Voltage, all inputs	V <sub>IH</sub>	V <sub>dd</sub> x .7	V <sub>dd</sub> x .5	V
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-0.6	V <sub>dd</sub> x .3	V
OUTPUT LOW VOLTAGE, I <sub>OUT</sub> = 3mA	V <sub>OL</sub>		0.4	V
INPUT LEAKAGE CURRENT, V <sub>IN</sub> = GND to V <sub>cc</sub>	I <sub>LI</sub>	0.10	3	µA
OUTPUT LEAKAGE CURRENT, V <sub>OUT</sub> = GND to V <sub>cc</sub>	I <sub>LO</sub>	0.05	3	µA
STANDBY CURRENT SCL=SDA=V <sub>cc</sub> -0.3V, All other inputs = GND or 3.3V +10%	I <sub>SB</sub>	1.6	4	µA
POWER SUPPLY CURRENT READ: SCL clock frequency = 100 KHz	I <sub>CCR</sub>	0.4	1	µA
POWER SUPPLY CURRENT WRITE: SCL clock frequency = 100 KHz	I <sub>CCW</sub>	2	3	µA

Continued:

**SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS** (VCC = +3.3V ± 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	tAA	0.2	0.9	μs	
Idle bus time before a transition can start	tBUF	1.3		μs	
Data-out hold time	tDH	200		ns	
SDA and SCL fall time	tF		300	ns	
Data-in hold time	tHD:DAT	0		μs	
Start condition hold time	tHD:STA	0.6		μs	
Clock HIGH period	tHIGH	0.6		μs	
Noise suppression time constant at SCL, SDA inputs	ti		50	ns	
Clock LOW period	tLOW	1.3		μs	
SDA and SCL rise time	tR		0.3	μs	
SCL clock frequency	tSCL		400	KHz	
Data-in setup time	tSU:DAT	100		ns	
Start condition setup time	tSU:STA	0.6		μs	
Stop condition setup time	tSU:STO	0.6		μs	
WRITE cycle time	tWRC		10	ms	1

**NOTES:** 1. The SPD EEPROM WRITE cycle time (tWR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

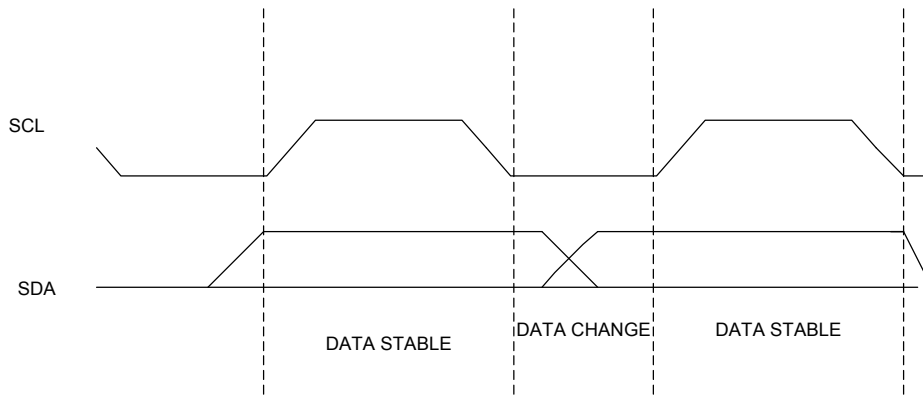


Figure 1  
DATA VALIDITY

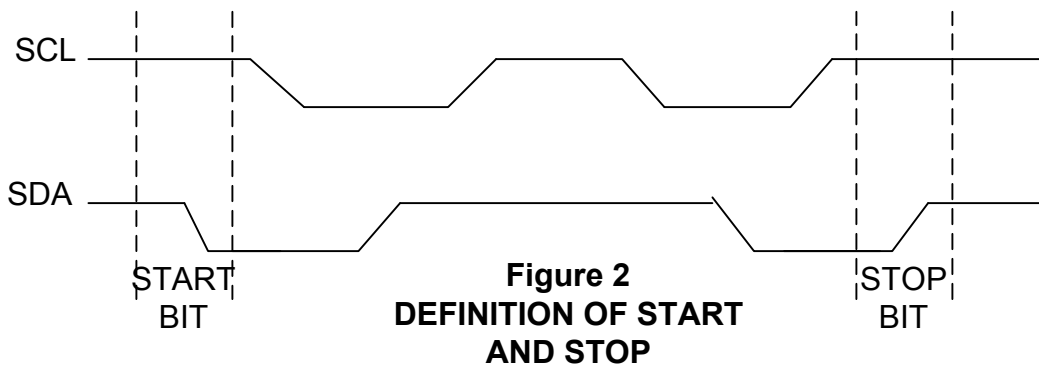


Figure 2  
DEFINITION OF START  
AND STOP

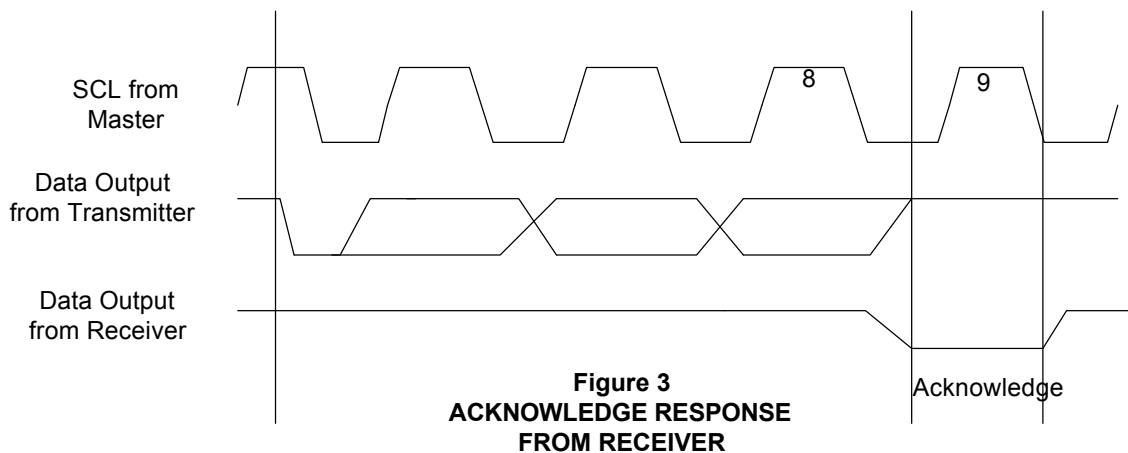


Figure 3  
ACKNOWLEDGE RESPONSE  
FROM RECEIVER