SDRAM DDR2 MODULE 128M, 256MX64 UDIMM

Features:

- ROHS Complaint
- 240 pin unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates PC2-4200, PC2-5300
- Utilizes DDR2-533 and DDR2-667 SDRAM FBGA components
- 1GB (128MX64), 2GB (256MBX64)
- Vdd = VddQ 1.8v ±0.1v,
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK0 and CK0#)
- 64ms, 8,182 cycle refresh
- 7.8125us maximum average periodic refresh interval
- Programmable burst lengths: 4 or 8
- SERIAL Presence Detect (SPD)

Options: Part Number:

8 - 128Mx8 DDR2 SDRAM FBGA PD128M6408U38Z-XX
PD128M6408U48B-XX

16 -128MX8 DDR2 SDRAM FBGA PD256M6416U38Z-XX
PD128M6416U48B-XX

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	CAS Latency
-37E	**-37E**	**267MHz**	**4**
-3	**-3**	**333MHz**	**5**

GENERAL DESCRIPTION

The P128M648(XXX), P256M6416(XXX) are high performance dynamic random-access 1GB and 2GB modules respectively. These modules are organized in a x64 configuration, and utilize quad bank architecture with a synchronous DDR interface. These DDR SDRAM modules use double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM DC RATINGS:

Voltage on Vdd Supply relative to Vss .....-1 to +2.3V
Voltage on VddQ Supply relative to Vss.....-0.5V to+2.3V
Voltage on VddL Supply relative to Vss.....-0.5V to+2.3V
Voltage on Vref and Inputs relative to Vss.....-1V to +3.6V
Voltage on I/O pins relative to Vss… -0.5V to VddQ +0.5V
Operating Temperature T_A (Ambient) .....0 ° to +85 °C
Storage Temperature.....-55 to +150 °C

PIN ASSIGNMENT
240-Pin UDIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vref	61	A4	121	VSS	181	VDDQ
2	Vss	62	VDDQ	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	VDD	124	VSS	184	VDD
5	Vss	65	VSS	125	DM0	185	CK0
6	DQSO#	66	VSS	126	NC	186	CK0#
7	DQS0	67	VDD	127	VSS	187	VDD
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10	130	VSS	190	BA1
11	Vss	71	BA0	131	DQ12	191	VDDQ
12	DQ8	72	VDDQ	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	VSS	193	S0#
14	Vss	74	CAS#	134	DM1	194	VDDQ
15	DQS1#	75	VDDQ	135	NC	195	ODT0
16	DQS1	76	NC	136	VSS	196	A13
17	Vss	77	NC	137	CK1	197	VDD
18	NC	78	VDDQ	138	CK1#	198	VSS
19	NC	79	VSS	139	VSS	199	DQ36
20	Vss	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	VSS	142	VSS	202	DM4
23	Vss	83	DQS4#	143	DQ20	203	NC
24	DQ16	84	DQS4	144	DQ21	204	VSS
25	DQ17	85	VSS	145	VSS	205	DQ38
26	Vss	86	DQ34	146	DM2	206	DQ39
27	DQS2#	87	DQ35	147	NC	207	VSS
28	DQS2	88	VSS	148	VSS	208	DQ44
29	Vss	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	VSS
31	DQ19	91	VSS	151	VSS	211	DM5
32	Vss	92	DQS5#	152	DQ28	212	NC
33	DQ24	93	DQS5	153	DQ29	213	VSS
34	DQ25	94	VSS	154	VSS	214	DQ46
35	Vss	95	DQ42	155	DM3	215	DQ47
36	DQS3#	96	DQ43	156	NC	216	VSS
37	DQS3	97	VSS	157	VSS	217	DQ52
38	Vss	98	DQ48	158	DQ30	218	DQ53
39	Dq26	99	DQ49	159	DQ31	219	VSS
40	Dq27	100	VSS	160	VSS	220	CK2
41	Vss	101	SA2	161	NC	221	CK2#
42	NC	102	NC	162	NC	222	VSS
43	NC	103	VSS	163	VSS	223	DM6
44	Vss	104	DQS6#	164	NC	224	NC
45	NC	105	DQS6	165	NC	225	VSS
46	NC	106	VSS	166	VSS	226	DQ54
47	Vss	107	DQ50	167	NC	227	DQ55
48	NC	108	DQ51	168	NC	228	VSS
49	NC	109	VSS	169	VSS	229	DQ60
50	Vss	110	DQ56	170	VDDQ	230	DQ61
51	VDDQ	111	DQ57	171	NC	231	VSS
52	CKE0	112	VSS	172	VDD	232	DM7
53	VDD	113	DQS7#	173	NC	233	NC
54	BA2	114	DQS7	174	NC	234	VSS
55	NC	115	VSS	175	VDDQ	235	DQ62
56	VDDQ	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	VSS
58	A7	118	VSS	178	VDD	238	VDDSPD
59	VDD	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

Rev: 04/04/07

Spectek Module Part Options and Designations

Options	Designation
Spectek Module	PD
Module Depth & Width	
1GB	128M64
2GB	256M64
2 Digit chip count	
8 Chips	08
16 chips	16
Design ID	
Design revision	U38Z
	U48B
Module type	
UDIMM	D
Component type	
X8	2
X16	3
Package Type	
Lead Free FBGA	J
Leaded FBGA	B
Lead Free TSOP	Z
Leaded TSOP	T
Module Speed Grade	
DDR2 533 PC2-4200	-37E
DDR2 667 PC2-5300	-3

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:

Parameter		Symbol	Min	Nom	Max	Units
Supply Voltage		Vdd	1.7	1.8	1.9	V
VDDL Supply Voltage		VDDL	1.7	1.8	1.9	V
I/O Supply Voltage		VddQ	1.7	1.8	1.9	V
I/O Reference Voltage		Vref	0.49 x VddQ	0.50 xVddQ	0.51 X VddQ	V
I/O Termination Voltage (system)		Vtt	Vref – 0.04		Vref + 0.04	V
Input Leakage Current Any input = 0V ≤ VIN ≤ Vdd All other pins not under test = 0V	Command/Address WE#, RAS#, CAS#, CKE, S#	I_I	-40		40	uA
	CK0, CK0#	I_I	-10		10	uA
	CK1, CK1#, CK2, CK2#	I_I	-15		15	uA
	DM	I_I	-5		5	uA
Output Leakage Current DQs are disabled; 0V ≤ VOUT ≤ VddQ		I_{OZ}	-5		5	uA
Vref Leakage Current; Vref = Valid Vref level		Ivref	-16		16	uA

AC INPUT OPERATING CONDITIONS: (This parameter is sampled. Vdd = +1.8V ± 0.1V, VddQ = +1.8V ±0.1V)

Parameter	Symbol	MIN	MAX	Units
Input High (Logic 1) Voltage	VIH (AC)	Vref +0.250		V
Input Low (Logic 0) Voltage (-37E)	VIL (AC)		Vref +0..250	V
Input Low (Logic 0) Voltage (-3)	VIL (AC)		Vref +0..200	V

DC INPUT OPERATING CONDITIONS: (This parameter is sampled. Vdd = +1.8V ± 0.1V, VddQ = +1.8V ±0.1V)

Parameter	Symbol	MIN	MAX	Units
Input High (Logic 1) Voltage	VIH (DC)	Vref +0.125	VddQ + .300	V
Input Low (Logic 0) Voltage	VIL (DC)	-.300	Vref +0..125	V

IDD OPERATING CONDITIONS AND MAXIMUM LIMITS: Vdd = Q1.8V ± .1V, Temp. = 0° to 85 °C

Supply Current	Symbol		-3	-37E	Units

Operating on device bank active-precharge current: Tck=tck (IDD), trc=trc(IDD), tras=tras MIN(idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	Idd0	1GB 2GB	680 720	640 680	mA mA
Operating one device bank active-read-precharge current: Iout=0mA; BL=4, CL=CL(IDD), AL=0; tck=tck(IDD), trc=trc(IDD), tras=tras MIN(IDD), trcd=trcd(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	Idd1	1GB 2GB	800 TBD	760 TBD	mA mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; tck=tck(IDD) CKE is LOW, Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Idd2P	1GB 2GB	78.4 156.8	78.4 156.8	mA mA
Precharge quiet standby current: All device banks Idle; Tck = Tck(IDD) CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Idd2Q	1GB 2GB	440 880	328 656	mA mA
PRECHARGE STANDBY CURRENT: All device banks idle: tck = tck(IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching Data bus inputs are switching	Idd2N	1GB 2GB	480 960	360 720	mA mA
ACTIVE POWER DOWN CURRENT; All device banks open; tck = tck(IDD) CKE is LOW; Other control and address bus inputs are STABLE; Data bus input are FLOATING	Idd3P	1GB 2GB	320 640	280 560	mA mA
ACTIVE STANDBY CURRENT: All device banks open; tck=tck(IDD), tras=tras MAX (IDD) trp=trp(IDD); CKE is HIGH,S# is HIGH between valid commands; other control and address bus inputs are switching; Data bus inputs are switching.	Idd3N	1GB 2GB	560 1120	440 880	mA mA
OPERATING BURST WRITE CURRENT; All device banks open, Continuous burst writes; BL=4, CL=CL(IDD), AL=0; tck-tck(IDD), tras=tras MAX(IDD), trp = trp(IDD); CKE is HIGH, S# is HIGH, S# is HIGH between valid commands; Address bus inputs are switching, Data bus inputs are switching	Idd4W	1GB 2GB	1280 1358.4	1040 1118.4	mA mA
OPERATING BURST READ CURRENT: All device banks open, Continuous burst reads, Iout = 0Ma; BL=4, CL=CL(IDD), AL=0, tck=tck (IDD), tras=tras MAX(IDD), trp=trp(IDD), CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	Idd4R	1GB 2GB	1280 1358.4	1160 1238.4	mA mA
Burst refresh currenl: tck=tck(IDD): Refresh command at every trfc(IDD) interval; CKE is HIGH, S# is HIGH between volid commands; Other control and address bus inputs are switching; Data bus inputs are swiching	Idd5	1GB 2GB	2160 4320	2000 4000	mA mA
Operating device bank interleave read current: All device banks interleaving reads, Iout=0mA.BL=4, CL=CL(IDD), AL=trcd (IDD)-1 X tck(IDD); tck=tck(IDD), trc=trc(IDD), trrd=trrd(IDD), trcd =trcd(IDD), CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are switching.	Idd7	1GB 2GB	2000 2456	1820 2376	mA mA

NOTES:

AC ELECTRICAL CHARACTERISTICS: Vdd = 1.8 +/-.1V; Temp. = 0° to 85°C

AC CHARACTERISTICS: CLOCK and DATA			-3		-37E		
PARAMETER		**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Clock cycle time	CL=5	tCK	3.0	8.0			ns
	CL=4	tCK	3.75	8.0	3.75	8.0	ns
	CL=3	tCK	5.0	8.0	5.0	8.0	ns
CK high-level width		tCH	0.48	0.52	0.48	0.52	tCK
CK low-level width		tCL	0.48	0.52	0.48	0.52	tCK
Half clock period		tHP	tCH, tCL		tCH, tCL		ps
Clock Jitter		tJITTER	-125	125	-125	125	ps
DQ output access time from clock		tAC	-450	+450	-500	+500	ps
Data-out high-impedance window from clock		tHZ		tAC		tAC	ps
Data out low impedance window from clock		tLZ	tAC	tAC	tAC	tAC	ps
DQ and DM input setup time relative to DQS		tDSa	300		350		ps
DQ and DM input hold time relative to DQS		tDHa	300		350		ps
DQ and DM input setup time relative to DQS		tDSb	100		100		ps
DQ and DM input hold time relative to DQS		tDHb	175		225		ps
DQ and DM input pulse width (for each input)		tDIPW	0.35		0.35		tCK
Data hold skew factor		tQHS		340		400	ps
DQ-DQS hold, DQS to first DQ to go nonvalid, per access		tQH	tHP-tQHS		tHP-tQHS		ps
Data valid output window (DVW)		tDVW	tQH-tDQSQ		tQH-tDQSQ		ps
DQS input high pulse width		tDQSH	0.35		0.35		tCK
DQS input pulse width		tDQSL	0.35		0.35		tCK
DQS output access time from clock		tDQSCK	-400	+400	-450	+450	ps
DQS falling edge to CK rising –setup time		tDSS	0.2		0.2		tCK
DQS falling edge from CK rising – hold time		tDSH	0.2		0.2		tCK
DQS-DQ skew, DQS to last DQ valid, per group, per access		tDQSQ		240		300	ps
DQS read preamble		tRPRE	0.9	1.1	0.9	1.1	tCK
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	tCK
DQS write preamble setup time		tWPRES	0		0		ps
DQS write preamble		tWPRE	0.35		0.25		tCK
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	tCK
Write command to first DQS latching transition		tDQSS	WL-0.25	WL +0.25	WL-0.25	WL +0.25	tCK
Address and control input pulse width for each input		tIPW	0.6		0.6		tCK
Address and control input setup time		tISa	400		500		ps
Address and control input hold time		tIHa	400		500		ps
Address and control input setup time		tISb	200		250		ps
Address and control input hold time		tIHb	275		375		ps
CAS# to CAS# command delay		tCCD	2		2		tCK
ACTIVE to ACTIVE (SAME BANK) command		tRC	55		55		ns
ACTIVE bank a to active bank b command		tRRD	7.5		7.5		ns
ACTIVE to READ or WRITE delay		tRCD	15		15		ns
Four Bank Activate period		tFAW	37.5		37.5		ns
ACITVE to PRECHARGE command		tRAS	40	70,000	40	70,000	ns
Internal READ to precharge command delay		tRTP	7.5		7.5		ns
Write recovery time		tWR	15		15		ns
Auto precharge write recovery +precharge		tDAL	tWR +tRP		tWR +tRP		ns
Internal WRITE to READ command delay		tWTR	7.5		7.5		ns
PRECHARGE command period		tRP	15		15		ns
PRECHARGE ALL command period		tRPA	tRP + tCK		tRP + tCK		ns
LOAD MODE command cycle time		tMRD	2		2		tCK
CKE low to CK, CK# uncertainty		tDELAY	tIS+ tCK+ tIH		tIS+ tCK+ tIH		ns
REFRESH TO ACTIVE or REFRESH to REFRESH Command interval		tRFC	127.5	70,000	127.5	70,000	ns
Average periodic refresh interval		tREFI		7.8		7.8	us
Exit SELF REFRESH to non-READ command		tXSNR	tRFC (MIM)+10		tRFC (MIM)+10		ns
Exit SELF REFRESH to READ command		tXSRD	200		200		tCK
Exit SELF REFRESH timing reference		tISXR	tIS		tIS		ps

SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units
Supply Voltage	V_{CC}	1.7	3.6	V
Input High (Logic 1) Voltage, all inputs	V_{IH}	Vcc x .7	Vcc x .5	V
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.6	Vcc x .3	V
OUTPUT LOW VOLTAGE, I_{OUT} =3mA	V_{OL}		0.4	V
INPUT LEAKAGE CURRENT, V_{IN} = GND to Vcc	I_{LI}	0.10	3	µA
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to Vcc	I_{LO}	0.05	3	µA
STANDBY CURRENT SCL=SDA=Vcc -0.3V, All other inputs = GND or 3.3V +10%	I_{SB}	1.6	4	µA
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}	0.4	1	µA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	t_{AA}	0.2	0.9	µs	
Idle bus time before a transition can start	t_{BUF}	1.3		µs	
Data-out hold time	t_{DH}	200		ns	
SDA and SCL fall time	t_{F}		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		µs	
Start condition hold time	$t_{HD:STA}$	0.6		µs	
Clock HIGH period	t_{HIGH}	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	t_{I}		50	ns	
Clock LOW period	t_{LOW}	1.3		µs	
SDA and SCL rise time	t_{R}		0.3	µs	
SCL clock frequency	t_{SCL}		400	KHz	
Data-in setup time	$t_{SU:DAT}$	100		ns	
Start condition setup time	$t_{SU:STA}$	0.6		µs	
Stop condition setup time	$t_{SU:STO}$	0.6		µs	
WRITE cycle time	t_{WR}		10	ms	1

NOTES: 1. The SPD EEPROM WRITE cycle time (t_{WR}) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

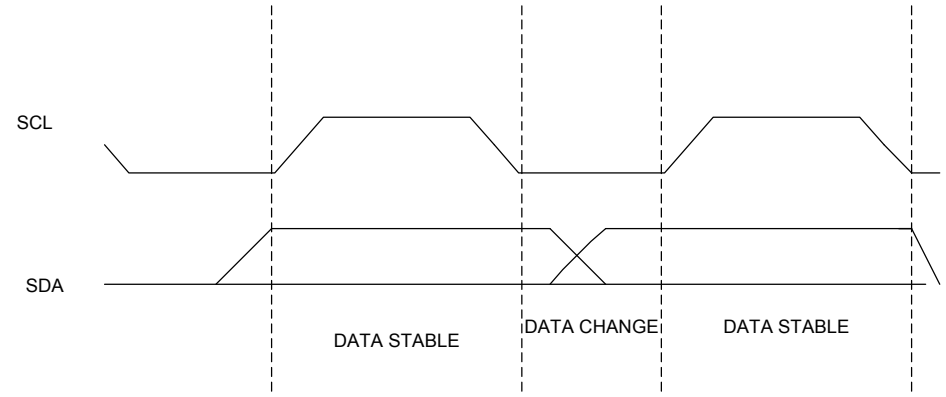

Figure 1
DATA VALIDITY

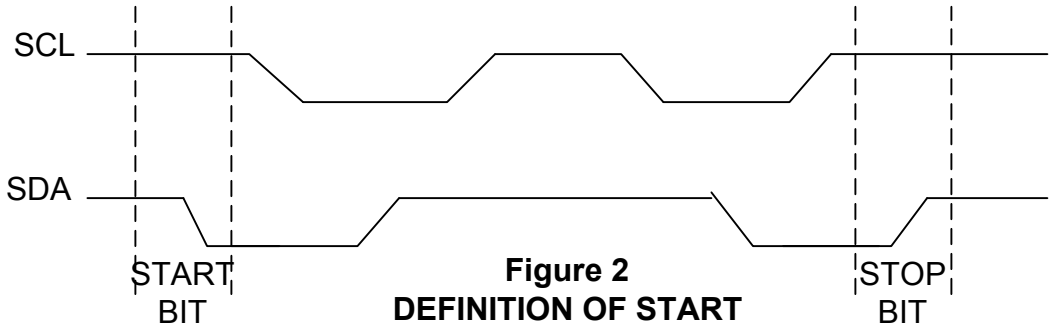

Figure 2
DEFINITION OF START AND STOP

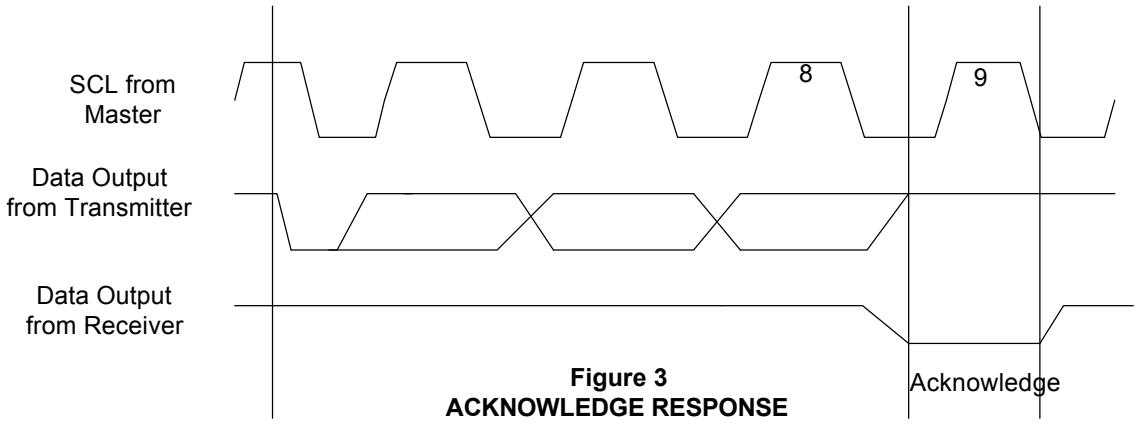

Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER