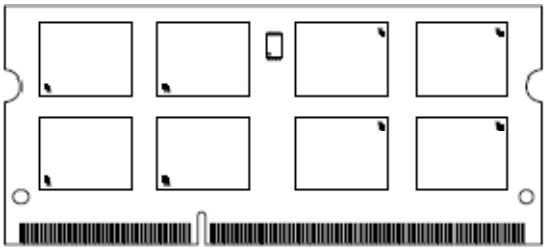
SDRAM DDR3 128M, 256M X 64 SODIMM

204-Pin SODIMM Assembly



Features:

- ROHS Complaint
- 204 pin small outline dual in-line memory module (SODIMM)
- Fast data transfer rates PC3-10600, PC3-8500
- Utilizes DDR3-1066 and DDR3-1333 SDRAM FBGA components
- 1GB (128MX64), 2GB (256MX64)
- Vdd = VddQ 1.5V ±0.75V,
- Adjustable data-output drive strength
- Addresses are mirrored for second rank
- 64ms, 8,182 cycle refresh
- 7.8125us maximum average periodic refresh interval
- Gold edge connector contacts
- SERIAL Presence Detect (SPD)

Options:

8 -128Mx8 DDR3 SDRAM FBGA CHIPS
P(X)128M6408V58BS2J-XX

16 - 128MX8 DDR3 SDRAM FBGA CHIPS
P(X)256M6416V58BS2J-XX

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	Latencies CL-trcd-trp
-18E	-18E	533MHz	7-7-7
-15E	-15E	667MHz	9-9-9

GENERAL DESCRIPTION

The P(X)128M6408V58BS2J and P(X)256M64V58BS2J are high performance dynamic random-access 1GB and 2GB modules respectively. These modules are organized in a x64 configuration, and utilize 8 bank architecture with a synchronous DDR interface. These DDR3 SDRAM modules use double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM DC RATINGS:

Voltage on Vdd Supply relative to Vss -1 to +2.3V
Voltage on VddQ Supply relative to Vss…..-0.5V to+2.3V
Voltage on VddL Supply relative to Vss…..-0.5V to+2.3V
Voltage on Vref and Inputs relative to Vss…..-1V to +3.6V
Voltage on I/O pins relative to Vss… -0.5V to VddQ +0.5V
Operating Temperature T_A (Ambient) .....0 ° to +85 °C
Storage Temperature.....-55 to +150 °C

Spectek Module Part Options and Designations

Options	Designation
Spectek Module	PD: Manufactured in USA PC: Manufactured in China PT: Manufactured in Tawian
Module Depth & Width	
1GB	128M64
2GB	256M64
2 Digit chip count	
8 Chips	08
16 chips	16
Design ID	
Design revision	V58B
Module type	
SODIMM	S
Component type	
X8	2
Package Type	
Lead Free FBGA	J
Leaded FBGA	B
Module Speed Grade	
DDR3 1066 PC3-8500	18E (187E)
DDR3 1333 PC3-10600	15E

204 pin SODIMM Pin Assignments

204-Pin DDR3 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	DQ19	105	V_{DD}	157	DQ42
3	V_{SS}	55	V_{SS}	107	A10	159	DQ43
5	DQ0	57	DQ24	109	BA0	161	V_{SS}
7	DQ1	59	DQ25	111	V_{DD}	163	DQ48
9	V_{SS}	61	V_{SS}	113	WE#	165	DQ49
11	DM0	63	DM3	115	CAS#	167	V_{SS}
13	V_{SS}	65	V_{SS}	117	V_{DD}	169	DQS6#
15	DQ2	67	DQ26	119	A13	171	DQS6
17	DQ3	69	DQ27	121	S1#	173	V_{SS}
19	V_{SS}	71	V_{SS}	123	V_{DD}	175	DQ50
21	DQ8	73	CKE0	125	NC	177	DQ51
23	DQ9	75	V_{DD}	127	V_{SS}	179	V_{SS}
25	V_{SS}	77	NC	129	DQ32	181	DQ56
27	DQS1#	79	BA2	131	DQ33	183	DQ57
29	DQS1	81	V_{DD}	133	V_{SS}	185	V_{SS}
31	V_{SS}	83	A12	135	DQS4#	187	DM7
33	DQ10	85	A9	137	DQS4	189	V_{SS}
35	DQ11	87	V_{DD}	139	V_{SS}	191	DQ58
37	V_{SS}	89	A8	141	DQ34	193	DQ59
39	DQ16	91	A5	143	DQ35	195	V_{SS}
41	DQ17	93	V_{DD}	145	V_{SS}	197	SA0
43	V_{SS}	95	A3	147	DQ40	199	V_{DDSPD}
45	DQS2#	97	A1	149	DQ41	201	SA1
47	DQS2	99	V_{DD}	151	V_{SS}	203	V_{TT}
49	V_{SS}	101	CK0	153	DM5	–	–
51	DQ18	103	CK0#	155	V_{SS}	–	–

204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	V_{SS}	54	V_{SS}	106	V_{DD}	158	DQ46
4	DQ4	56	DQ28	108	BA1	160	DQ47
6	DQ5	58	DQ29	110	RAS#	162	V_{SS}
8	V_{SS}	60	V_{SS}	112	V_{DD}	164	DQ52
10	DQS0#	62	DQS3#	114	S0#	166	DQ53
12	DQ50	64	DQS3	116	ODT0	168	V_{SS}
14	V_{SS}	66	V_{SS}	118	V_{DD}	170	DM6
16	DQ6	68	DQ30	120	ODT1	172	V_{SS}
18	DQ7	70	DQ31	122	NC	174	DQ54
20	V_{SS}	72	V_{SS}	124	V_{DD}	176	DQ55
22	DQ12	74	CKE1	126	V_{REFCA}	178	V_{SS}
24	DQ13	76	V_{DD}	128	V_{SS}	180	DQ60
26	V_{SS}	78	NC	130	DQ36	182	DQ61
28	DM1	80	NC/A14	132	DQ37	184	V_{SS}
30	RESET#	82	V_{DD}	134	V_{SS}	186	DQS7#
32	V_{SS}	84	A11	136	DM4	188	DQS7
34	DQ14	86	A7	138	V_{SS}	190	V_{SS}
36	DQ15	88	V_{DD}	140	DQ38	192	DQ62
38	V_{SS}	90	A6	142	DQ39	194	DQ63
40	DQ20	92	A4	144	V_{SS}	196	V_{SS}
42	DQ21	94	V_{DD}	146	DQ44	198	EVENT#
44	V_{SS}	96	A2	148	DQ45	200	SDA
46	DM2	98	A0	150	V_{SS}	202	SCL
48	V_{SS}	100	V_{DD}	152	DQS5#	204	V_{TT}
50	DQ22	102	CK1	154	DQS5	–	–
52	DQ23	104	CK1#	156	V_{SS}	–	–

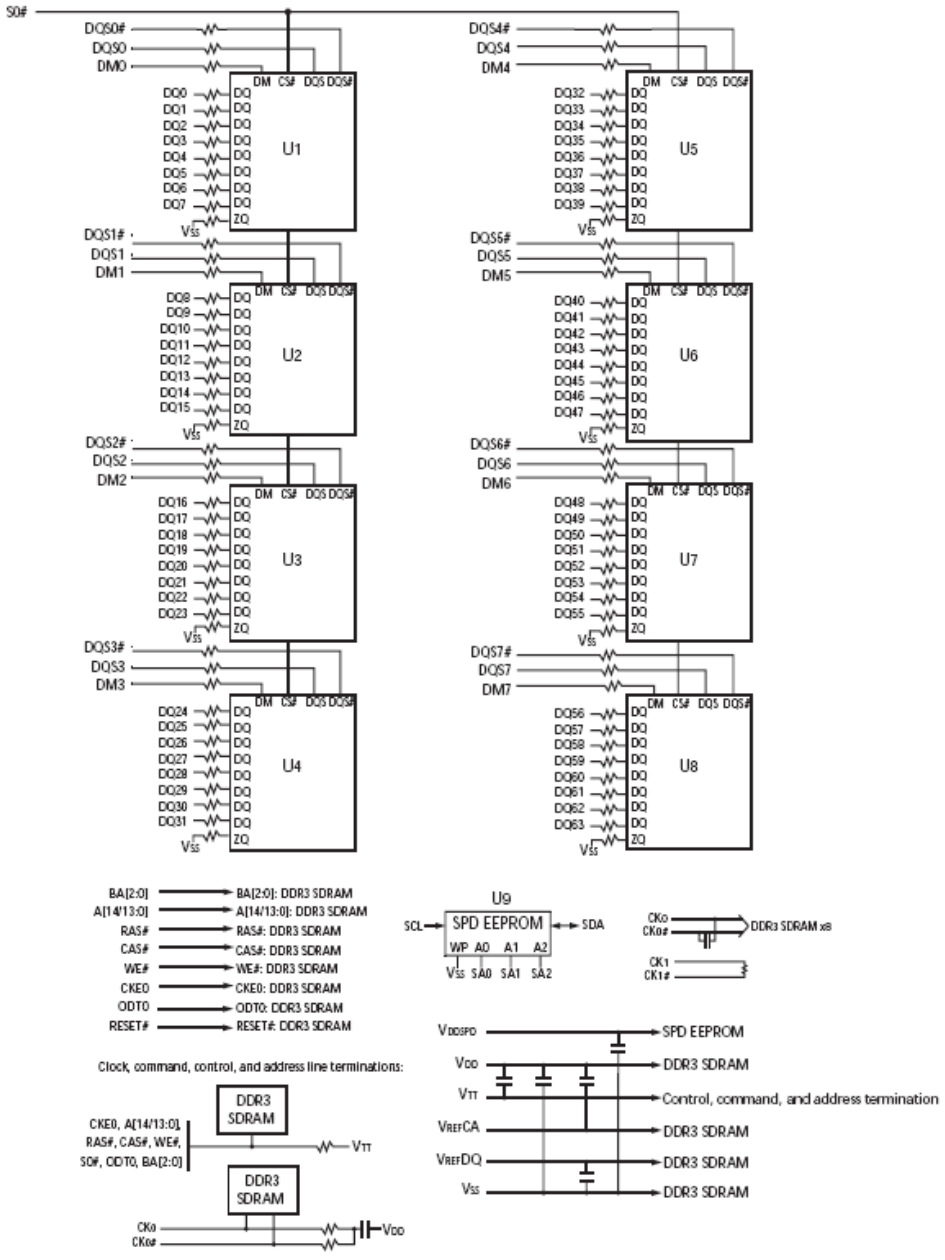
PIN DESCRIPTIONS

Symbol	Type	Description
A[14:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands. The address inputs also provide the op-code during the mode register command set. A[12:0] address the 1Gb DDR3 devices. A[13:0] address the 1Gb DDR3 devices. A[14:0] address the 2Gb DDR3 devices.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, and MR3) is loaded during the LOAD MODE command.
CK[1:0], CK#[1:0]	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DM[7:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of the DQS. Although the DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT[1:0]	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DD}. RESET# assertion and deassertion are asynchronous.
S#[1:0]	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA[1:0]	Input	**Presence-detect address inputs:** These pins are used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize communication to and from the temperature sensor/SPD EEPROM.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[7:0], DQS#[7:0]	I/O	**Data strobe:** DQS and DQS# are differential data strobes. Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the module on the I^2C bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.

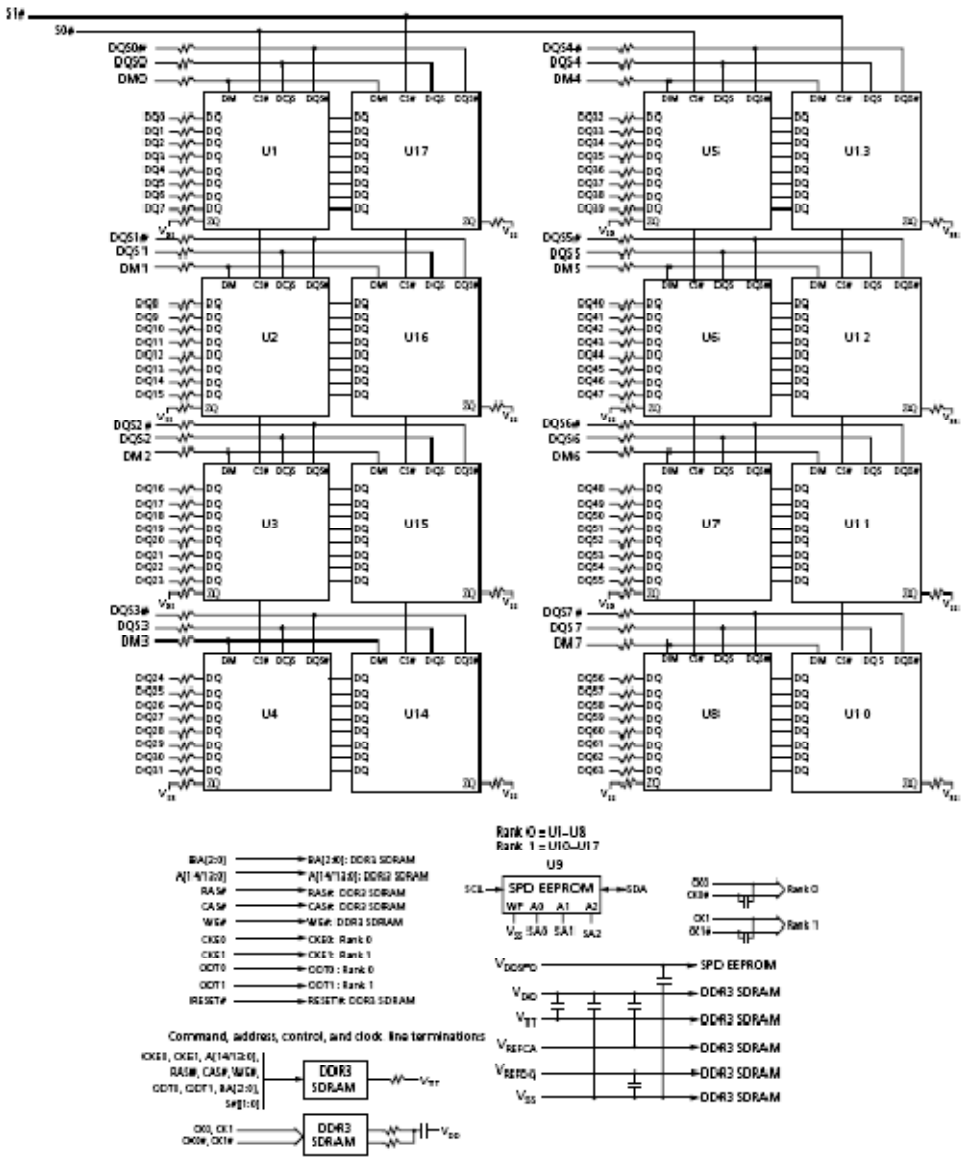
Pin Descriptions (Continued)

Symbol	Type	Description
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +3.0V to +3.6V. The component V_{DD} and V_{DDQ} are connected to the module Vdd.
V_{REFCA}	Supply	**Reference voltage:** Control, command, and address ($V_{DD}/2$).
V_{REFDQ}	Supply	**Reference voltage:** DQ, DM ($V_{DD}/2$).
V_{SS}	Supply	Ground.
V_{TT}	Supply	**Termination voltage:** Used for control, command, and address ($V_{DD}/2$).
NC	–	**No connect:** These pins are not connected on the module.

1GB Functional Block Diagram



2GB Functional Block Diagram



Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	+600	mA	
V_{TT}	Termination reference voltage – command address bus		0.483 x V_{DD}	0.5 x V_{DD}	0.517 x V_{DD}	V	1
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, BA	–32	0	+32	µA	
		S#, CKE, ODT, CK, CK#	–16	0	+16		
		DM	–4	0	+4		
I_{OZ}	Output leakage current: 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–10	0	+10	µA	
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–16	0	+16	µA	
T_A	Module ambient operating temperature	Commercial	0	–	+70	°C	2, 3
		Industrial	–40	–	+85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	+85	°C	2, 3, 4
		Industrial	–40	–	+95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

IDD Specifications

1GB DDR3 Idd Specifications and Conditions

Parameter	Symbol	1600	1333	1066	Units
Operating current 0: One bank ACTIVATE-to-PRE-CHARGE	I_{DD0}	960	880	800	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}	1120	1040	960	mA
Precharge power-down current: Slow exit	I_{DD2P}	96	96	96	mA
Precharge power-down current: Fast exit	I_{DD2P}	360	320	280	mA
Precharge quiet standby current	I_{DD2Q}	536	480	424	mA
Precharge standby current	I_{DD2N}	560	520	440	mA
Precharge standby ODT current	I_{DD2NT}	760	680	600	mA
Active power-down current	I_{DD3P}	360	320	280	mA
Active standby current	I_{DD3N}	536	496	456	mA
Burst read operating current	I_{DD4R}	2000	1600	1280	mA
Burst write operating current	I_{DD4W}	2000	1760	1520	mA
Refresh current	I_{DD5}	2080	1920	1760	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}	48	48	48	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}	72	72	72	mA
All banks interleaved read current	I_{DD7}	4800	3920	3120	mA
Reset current	I_{DD8}	112	112	112	mA

Addressing

Parameter	1GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128 Meg x 8)
Column address	1K A[9:0]
Module rank address	1 S0#

IDD Specifications

2GB DDR3 Idd Specifications and Conditions

Parameter	Symbol	1600	1333	1066	800	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	I_{DD0}[1]	1056	976	896	816	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	I_{DD1}[1]	1216	1136	1056	976	mA
Precharge power-down current: Slow exit	I_{DD2P}[2]	192	192	192	192	mA
Precharge power-down current: Fast exit	I_{DD2P}[2]	720	640	560	480	mA
Precharge quiet standby current	I_{DD2Q}[2]	1072	960	848	736	mA
Precharge standby current	I_{DD2N}[2]	1120	1040	880	800	mA
Precharge standby ODT current	I_{DD2NT}[2]	856	776	696	616	mA
Active power-down current	I_{DD3P}[2]	720	640	560	480	mA
Active standby current	I_{DD3N}[2]	1072	992	912	832	mA
Burst read operating current	I_{DD4R}[1]	2096	1696	1376	1136	mA
Burst write operating current	I_{DD4W}[1]	2096	1856	1616	1376	mA
Refresh current	I_{DD5B}[2]	4160	3840	3520	3200	mA
Self refresh temperature current: MAX T_C = 85°C	I_{DD6}[2]	96	96	96	96	mA
Self refresh temperature current (SRT-enabled): MAX T_C = 95°C	I_{DD6ET}[2]	144	144	144	144	mA
All banks interleaved read current	I_{DD7}[1]	4896	4016	3216	2896	mA
Reset current	I_{DD8}[2]	224	224	224	224	mA

Notes: 1. One module rank in the active I_{DD}; the other rank in I_{DD2P} (slow exit).
2. All ranks in this I_{DD} condition.

2GB Addressing

Parameter	2GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device page size per bank	1KB
Device configuration	1Gb (128 Meg x 8)
Column address	1K A[9:0]
Module rank address	2 S#[1:0]

SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units
Supply Voltage	V_{CC}	1.7	3.6	V
Input High (Logic 1) Voltage, all inputs	V_{IH}	Vcc x .7	Vcc x .5	V
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.6	Vcc x .3	V
OUTPUT LOW VOLTAGE, I_{OUT} =3mA	V_{OL}		0.4	V
INPUT LEAKAGE CURRENT, V_{IN} = GND to Vcc	I_{LI}	0.10	3	µA
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to Vcc	I_{LO}	0.05	3	µA
STANDBY CURRENT SCL=SDA=Vcc -0.3V, All other inputs = GND or 3.3V +10%	I_{SB}	1.6	4	µA
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}	0.4	1	µA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	t_{AA}	0.2	0.9	µs	
Idle bus time before a transition can start	t_{BUF}	1.3		µs	
Data-out hold time	t_{DH}	200		ns	
SDA and SCL fall time	t_{F}		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		µs	
Start condition hold time	$t_{HD:STA}$	0.6		µs	
Clock HIGH period	t_{HIGH}	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	t_{I}		50	ns	
Clock LOW period	t_{LOW}	1.3		µs	
SDA and SCL rise time	t_{R}		0.3	µs	
SCL clock frequency	t_{SCL}		400	KHz	
Data-in setup time	$t_{SU:DAT}$	100		ns	
Start condition setup time	$t_{SU:STA}$	0.6		µs	
Stop condition setup time	$t_{SU:STO}$	0.6		µs	
WRITE cycle time	t_{WR}		10	ms	1

NOTES: 1. The SPD EEPROM WRITE cycle time (t_{WR}) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

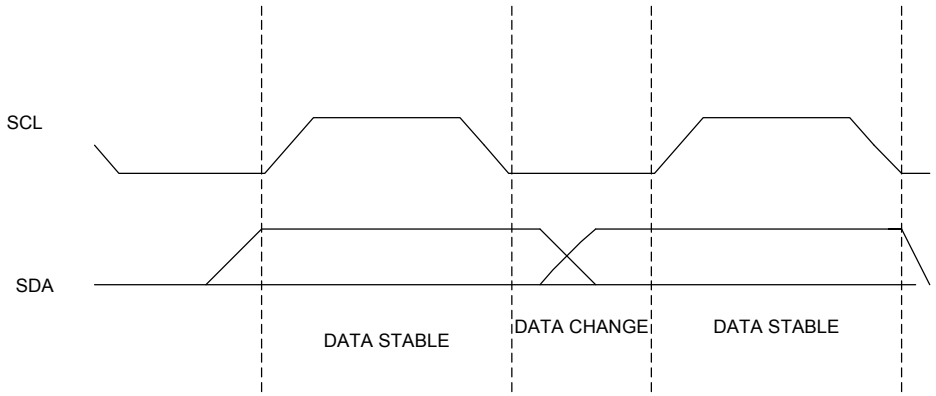


Figure 1
DATA VALIDITY

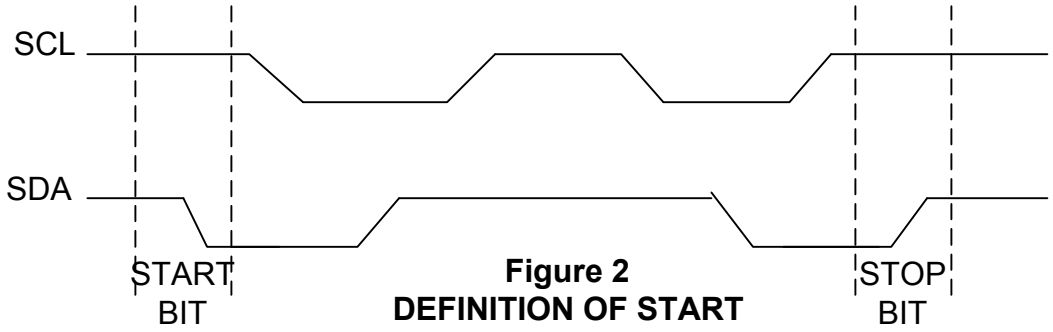


Figure 2
DEFINITION OF START AND STOP

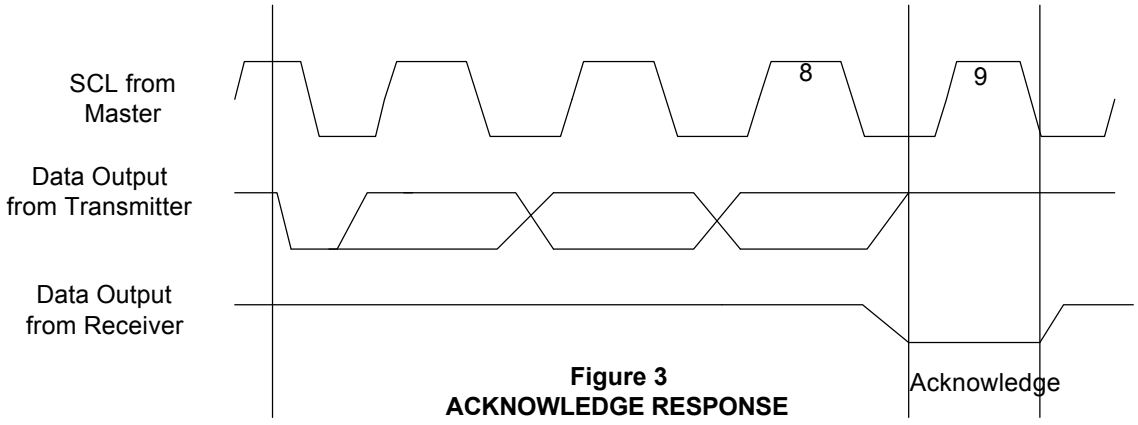


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

