SDRAM DDR3 128M, 256M X 64 UDIMM

Features:

- ROHS Compliant
- 240 pin unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates PC3-10600, PC3-8500
- Utilizes DDR3-1066 and DDR3-1333 SDRAM FBGA components
- 1GB (128MX64), 2GB (256MBX64)
- Vdd = VddQ 1.5v ±0.75V,
- Adjustable data-output drive strength
- Addresses are mirrored for second rank
- 64ms, 8,182 cycle refresh
- 7.8125us maximum average periodic refresh interval
- Gold edge connector contacts
- SERIAL Presence Detect (SPD)

Options:

8 -128Mx8 DDR3 SDRAM FBGA

16 - 128MX8 DDR3 SDRAM FBGA

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	Latencies CL-trcd-trp
-18E	**-18E**	**533MHz**	**7-7-7**
-15E	**-15E**	**667MHz**	**9-9-9**

GENERAL DESCRIPTION

The PX128M6408(XXX) and PX256M6416(XXX) are high performance dynamic random-access 1GB and 2GB modules respectively. These modules are organized in a x64 configuration, and utilize quad bank architecture with a synchronous DDR interface. These DDR SDRAM modules use double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM DC RATINGS:

Voltage on Vdd Supply relative to Vss.....-1 to +2.3V
Voltage on VddQ Supply relative to Vss…..-0.5V to+2.3V
Voltage on VddL Supply relative to Vss…..-0.5V to+2.3V
Voltage on Vref and Inputs relative to Vss…..-1V to +3.6V
Voltage on I/O pins relative to Vss… -0.5V to VddQ +0.5V
Operating Temperature T_A (Ambient) .....0 ° to +85 °C
Storage Temperature.....-55 to +150 °C

PIN ASSIGNMENT
240-Pin UDIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vrefdq	61	A2	121	Vss	181	A1
2	Vss	62	Vdd	122	DQ4	182	Vdd
3	DQ0	63	CK1	123	DQ5	183	Vdd
4	DQ1	64	CK1#	124	Vss	184	CK0
5	Vss	65	Vdd	125	DM0	185	CK0#
6	DQSO#	66	Vdd	126	NC	186	Vdd
7	DQS0	67	Vrefca	127	Vss	187	NC
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	Vdd	129	DQ7	189	Vdd
10	DQ3	70	A10	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	Vdd
12	DQ8	72	Vdd	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	S0#
14	Vss	74	CAS#	134	DM1	194	Vdd
15	DQS1#	75	Vdd	135	NC	195	ODT0
16	DQS1	76	S1#	136	Vss	196	A13
17	Vss	77	ODT1	137	DQ14	197	Vdd
18	DQ10	78	Vdd	138	DQ15	198	NC
19	DQ11	79	NC	139	Vss	199	Vss
20	Vss	80	Vss	140	DQ20	200	DQ36
21	DQ16	81	DQ32	141	DQ21	201	DQ37
22	DQ17	82	DQ33	142	Vss	202	Vss
23	Vss	83	Vss	143	DM2	203	DM4
24	DQS2#	84	DQS4#	144	NC	204	NC
25	DQS2	85	DQS4	145	Vss	205	Vss
26	Vss	86	Vss	146	DQ22	206	DQ38
27	DQ18	87	DQ34	147	DQ23	207	DQ39
28	DQ19	88	DQ35	148	Vss	208	Vss
29	Vss	89	Vss	149	DQ28	209	DQ44
30	DQ24	90	DQ40	150	DQ29	210	DQ45
31	DQ25	91	DQ41	151	Vss	211	Vss
32	Vss	92	Vss	152	DM3	212	DM5
33	DQS3#	93	DQS5#	153	NC	213	NC
34	DQS3	94	DQS5	154	Vss	214	Vss
35	Vss	95	Vss	155	DQ30	215	DQ46
36	DQ26	96	DQ42	156	DQ31	216	DQ47
37	DQ27	97	DQ43	157	Vss	217	Vss
38	Vss	98	Vss	158	NC	218	DQ52
39	NC	99	DQ48	159	NC	219	DQ53
40	NC	100	DQ49	160	Vss	220	Vss
41	Vss	101	Vss	161	NC	221	DM6
42	NC	102	DQS6#	162	NC	222	NC
43	NC	103	DQS6	163	Vss	223	Vss
44	Vss	104	Vss	164	NC	224	DQ54
45	NC	105	DQ50	165	NC	225	DQ55
46	NC	106	DQ51	166	Vss	226	Vss
47	Vss	107	Vss	167	NC	227	DQ60
48	NC	108	DQ56	168	RESET#	228	DQ61
49	NC	109	DQ57	169	CKE1	229	Vss
50	CKE0	110	Vss	170	Vdd	230	DM7
51	VDD	111	DQS7#	171	NC	231	NC
52	BA2	112	DQS7	172	NC	232	Vss
53	NC	113	Vss	173	Vdd	233	DQ62
54	Vdd	114	DQ58	174	A12	234	DQ63
55	A11	115	DQ59	175	A9	235	Vss
56	A7	116	Vss	176	Vdd	236	Vddpd
57	Vdd	117	SA0	177	A8	237	SA1
58	A5	118	SCL	178	A6	238	SDA
59	A4	119	SA2	179	Vdd	239	Vss
60	Vdd	120	Vtt	180	A3	240	Vtt

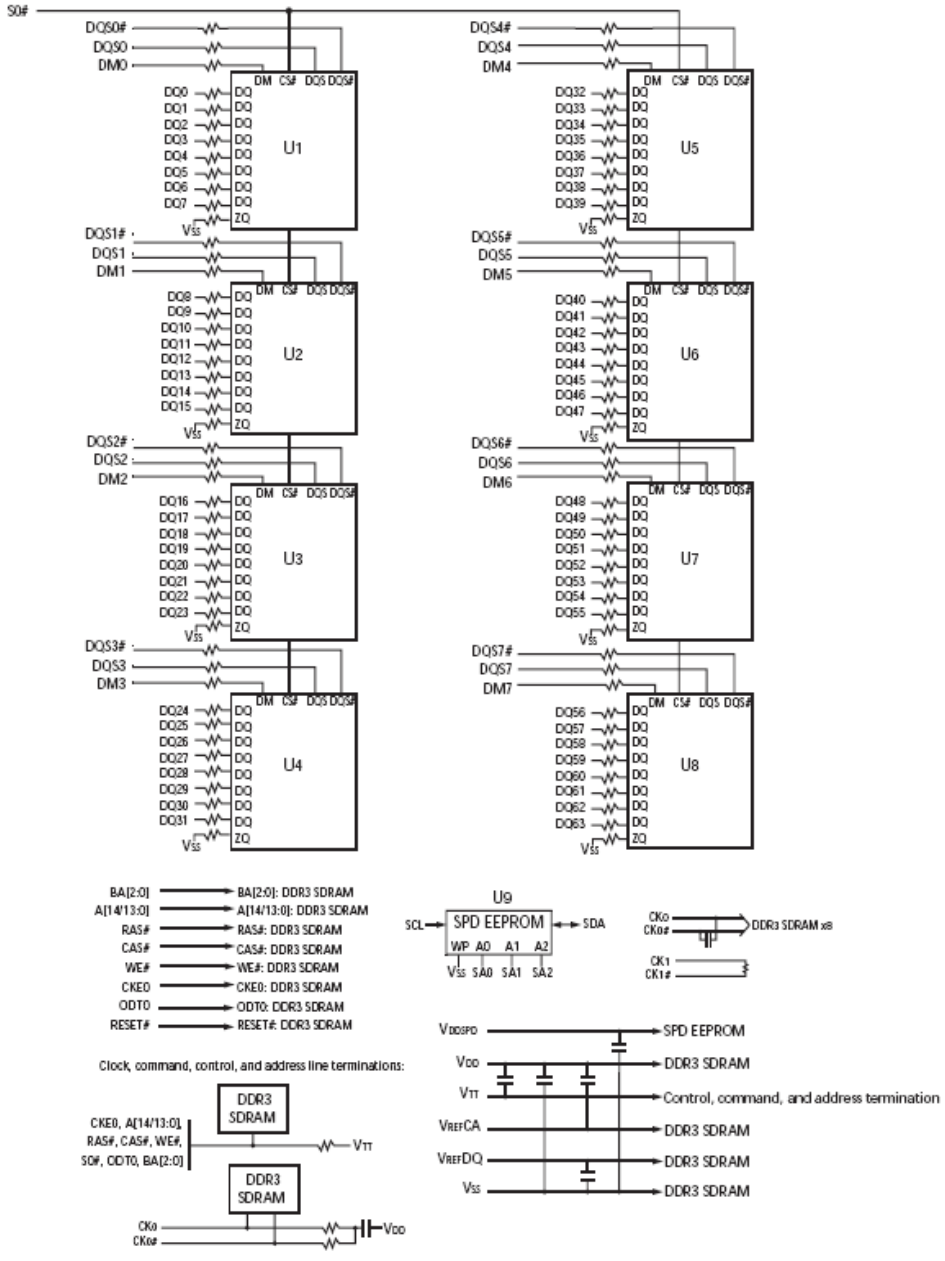
Spectek Module Part Options and Designations

Options	Designation
Spectek Module	PD
Module Depth & Width	
1GB	128M64
2GB	256M64
2 Digit chip count	
8 Chips	08
16 chips	16
Design ID	
Design revision	V48C V58B V68A
Module type	
UDIMM	D
Component type	
X8	2
Package Type	
Lead Free FBGA	J
Leaded FBGA	B
Module Speed Grade	
DDR3 1066 PC3-8500	18E (187E)
DDR3 1333 PC3-10600	15E

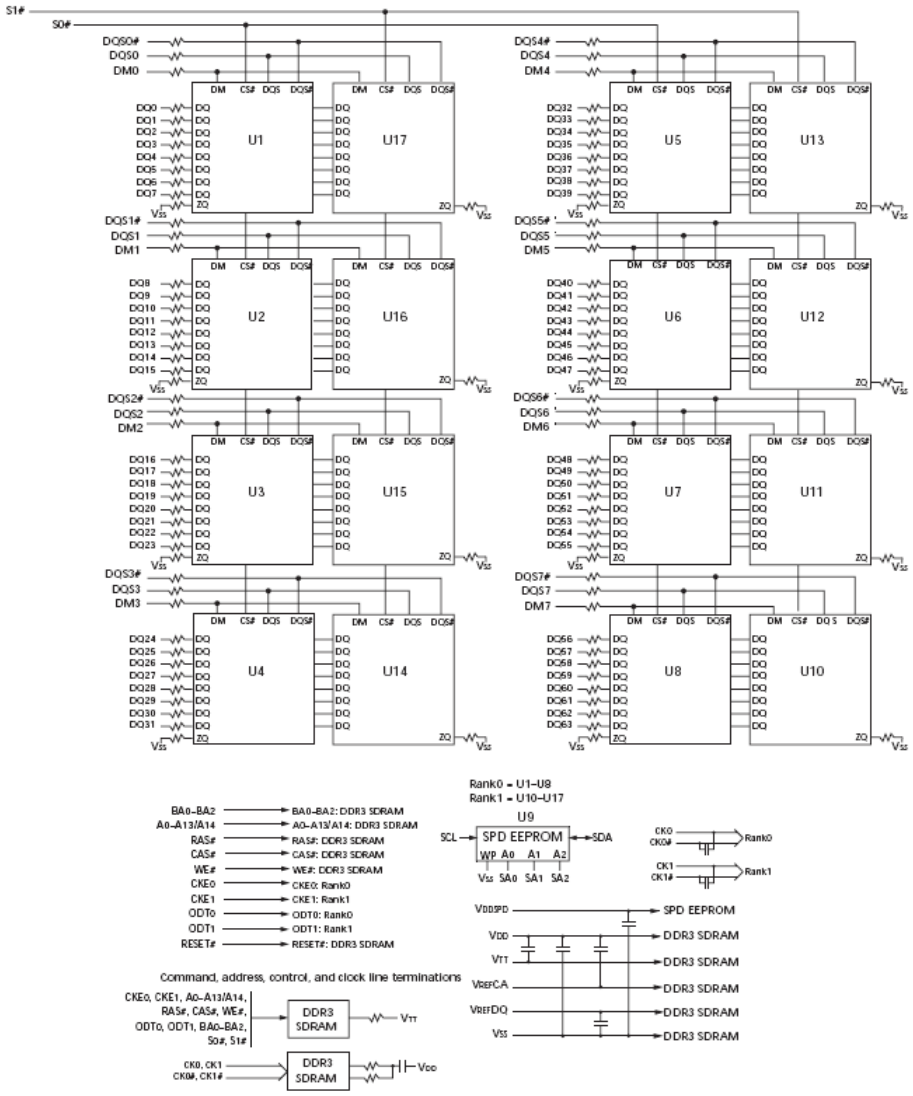
PIN DESCRIPTIONS

Symbol	Type	Description
A[14:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also used for BC4/BL8 identification as "BL on-the-fly" during CAS commands.. The address inputs also provide the op-code during the mode register command set. A[13:0] (1GB), A[14:0] (2GB).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the device bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command.
CK[1:0], CK0#[1:0]	Input	**Clock:** CK0 and CK0# are differential clock inputs. All contorl, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQ and DQS/DQS#) is referenced to the crossings of CK and CK#. CK1, CK1# are terminated.
CKE0	Input	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR3 SDRAM.
DM[7:0]	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of the DQ and DQS pins.
ODT0	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS,DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input and is defined as a rail-to-rail signal with DC HIGH ≥ 0.8 x VDD and DC LOW ≤ 0.2 x VDD. RESET# assertion and desertion are asynchronous.
SA[2:0]	Input	**Presence-detect address inputs:** These pins are used to configure the SPD EEPROM address range.
SCL	Input	**Serial clock for presence-detect:** SCL is used to synchronize presence-detect data transfer to and from the module.
S0#	Input	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder. With both inputs HIGH, all outputs of the register(s) are disabled except for CKE and ODT. CKE, ODT and chip select remain in previous state when both outputs are high.
DQ[63:0]	I/O	**Data input/output:** Bidirectional data bus.
DQS[7:0], DQS#[7:0]	I/O	**Data strobe:** Output with read data. Input with write data for source-synchronous operation. Edge-aligned with read data. Center-aligned with write data. DQS# is only used when the differential data strobe mode is enabled via the LOAD MODE command.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module.
VDD	Supply	**Power supply:** 1.5V ±0.075V.
VDDSPD	Supply	**Serial EEPROM positive power supply:** +3.0V to +3.6V.
VREFDQ	Supply	**Reference voltage:** DQ, DM (VDD/2).
VREFCA	Supply	**Reference voltage:** Control, command, and address (VDD/2).
Vss	Supply	Ground.
VTT	Supply	**Termination voltage:** Used for control, command, and address (VDD/2).
NC	–	**No connect:** These pins are not connected on the module.

1GB Functional Block Diagram



2GB Functional Block Diagram



DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:

Parameter		Symbol	Min	Nom	Max	Units
Supply Voltage		Vdd	1.425	1.5	1.575	V
Termination reference current from Vtt		Ivtt	-600	-	+600	
Termination reference voltage – command address bus		Vtt	+0.483 x Vdd	0.5 x Vdd	+0.517 x Vdd	V
Input Leakage Current Any input = 0V ≤ VIN ≤ Vdd Vref input 0V ≤ Vin ≤ 0.95V (All oht4r pins not under test = 0V)	Command/Address WE#, RAS#, CAS#, BA	I_I	-32	0	+32	uA
	S#, CKE, ODT, CK. CK#	I_I	-16	0	+16	uA
	DM	I_I	-5	0	+4	uA
Output leakage current: 0V ≤ Vout ≤ Vddq: DQs and ODT are disabled	DQ, DQS, DQS#	Ioz	-10	0	+10	uA
Output Leakage Current DQs are disabled; 0V ≤ VOUT ≤ VddQ		Ivref	-16	0	+16	uA

IDD OPERATING CONDITIONS AND MAXIMUM LIMITS: Vdd = Q1.5V ± .75V, Temp. = 0° to 70 °C

Supply Current	Symbol		-15E	-18E	Units
Operating on device bank active-precharge current: Tck=tck(IDD), trc=trc(IDD), tras=tras MIN(idd); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching.	Idd0	1GB 2GB	880 960	800 880	mA mA
Operating one device bank active-read-precharge current: Iout=0mA; BL=4, CL=CL(IDD), AL=0; tck=tck(IDD), trc=trc(IDD), tras=tras MIN(IDD), trcd=trcd(IDD); CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	Idd1	1GB 2GB	1040 1120	960 1040	mA mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; tck=tck(IDD) CKE is LOW, Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Idd2P	1GB 2GB	80 160	80 160	mA mA
Precharge quiet standby current: All device banks Idle; Tck = Tck(IDD) CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Idd2Q	1GB 2GB	480 960	424 848	mA mA
IDLE STANDBY CURRENT: All device banks idle: tck = tck(IDD); CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching Data bus inputs are switching	Idd2N	1GB 2GB	520 1040	440 880	mA mA
ACTIVE POWER DOWN STANDBY CURRENT; All device banks open; tck = tck(IDD) CKE is LOW; Other control and address bus inputs are STABLE; Data bus input are FLOATING	Idd3P	1GB 2GB	320 640	280 560	mA mA
ACTIVE STANDBY CURRENT: All device banks open; tck=tck(IDD), tras=tras MAX (IDD) trp=trp(IDD); CKE is HIGH,S# is HIGH between valid commands; other control and address bus inputs are switching; Data bus inputs are switching.	Idd3N	1GB 2GB	496 992	456 912	mA mA
OPERATING BURST WRITE CURRENT; All device banks open, Continuous burst writes; BL=4, CL=CL(IDD), AL=0; tck-tck(IDD), tras=tras MAX(IDD), trp = trp(IDD); CKE is HIGH, S# is HIGH, S# is HIGH between valid commands; Address bus inputs are switching, Data bus inputs are switching	Idd4W	1GB 2GB	1760 1840	1520 1600	mA mA
OPERATING BURST READ CURRENT: All device banks open, Continuous burst reads, Iout = 0Ma; BL=4, CL=CL(IDD), AL=0, tck=tck (IDD), tras=tras MAX(IDD), trp=trp(IDD), CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	Idd4R	1GB 2GB	1600 1680	1280 1360	mA mA
Burst refresh currenl: tck=tck(IDD): Refresh command at every trfc(IDD) interval; CKE is HIGH, S# is HIGH between volid commands; Other control and address bus inputs are switching; Data bus inputs are swiching	Idd5	1GB 2GB	1920 3840	1760 3520	mA mA
Operating device bank interleave read current: All device banks interleaving reads, Iout=0mA.BL=4, CL=CL(IDD), AL=trcd (IDD)-1 X tck(IDD); tck=tck(IDD), trc=trc(IDD), trrd=trrd(IDD), trcd =trcd(IDD), CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are switching.	Idd7	1GB 2GB	3920 4000	3120 3200	mA mA

NOTES:

SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units
Supply Voltage	V_{CC}	1.7	3.6	V
Input High (Logic 1) Voltage, all inputs	V_{IH}	Vcc x .7	Vcc x .5	V
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.6	Vcc x .3	V
OUTPUT LOW VOLTAGE, I_{OUT} =3mA	V_{OL}		0.4	V
INPUT LEAKAGE CURRENT, V_{IN} = GND to Vcc	I_{LI}	0.10	3	µA
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to Vcc	I_{LO}	0.05	3	µA
STANDBY CURRENT SCL=SDA=Vcc -0.3V, All other inputs = GND or 3.3V +10%	I_{SB}	1.6	4	µA
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}	0.4	1	µA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	
Idle bus time before a transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	
Data-in hold time	^{T}HD:DAT	0		µs	
Start condition hold time	^{T}HD:STA	0.6		µs	
Clock HIGH period	^{t}HIGH	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	
SCL clock frequency	^{t}SCL		400	KHz	
Data-in setup time	^{T}SU:DAT	100		ns	
Start condition setup time	^{T}SU:STA	0.6		µs	
Stop condition setup time	^{T}SU:STO	0.6		µs	
WRITE cycle time	^{t}WR		10	ms	1

NOTES: 1. The SPD EEPROM WRITE cycle time (^{t}WR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

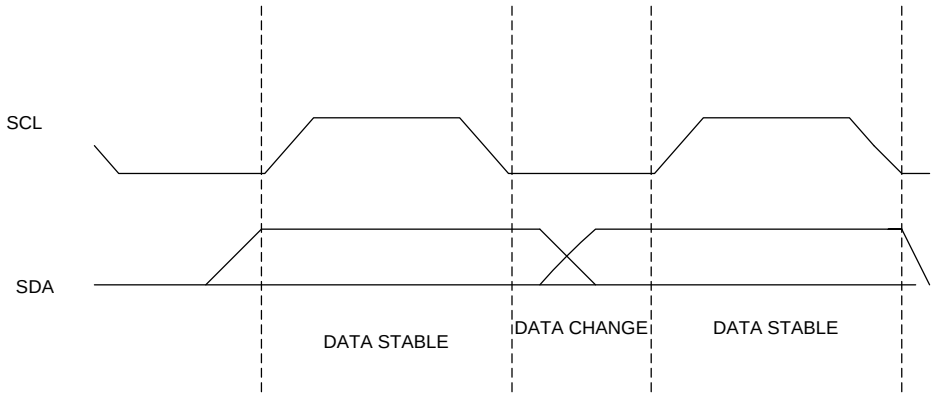


Figure 1
DATA VALIDITY

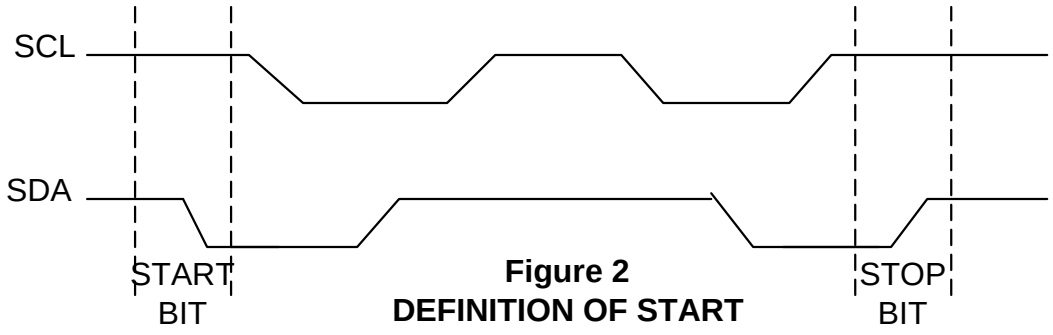


Figure 2
DEFINITION OF START AND STOP

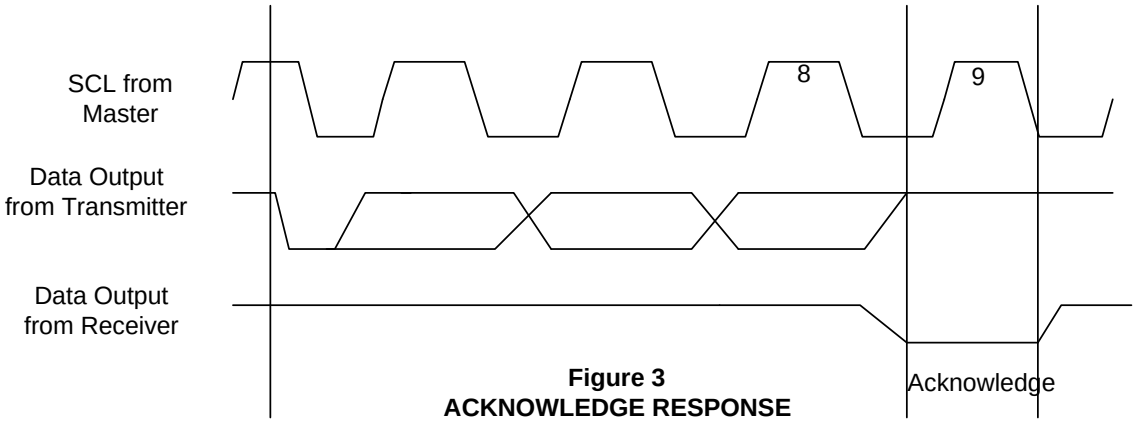


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

