PD32M6408 (XXX) D2X, PD64M6416 (XXX) D2X

SDRAM DDR MODULE 32M, 64M X 64 DIMM

Features:

- 184 pin dual in-line memory modules (DIMM)
- Fast data transfer rates PC2100, PC2700, PC3200
- Utilizes DDR266, DDR333 and DDR400B DDR SDRAM components
- 66p TSOP components.
- 256MB (32MX64), 512MB (64MX64)
- Vdd = 2.5v ±0.2v, VddQ = 2.5v ±0.2v
- 2.5v I/O (SSTL_2 compatible)
- Internal pipelined double data rate (DDR) Architecture, two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ Received with data
- Differential clock inputs (CK0 and CK0#)
- 7.8125us maximum average periodic refresh interval
- Programmable burst lengths: 2, 4 or 8

Options: Part Number:

8 - 32Mx8 DDR SDRAM TSOP	PD32M6408T16AD2T
	PD32M6408T26AD2T
	PD32M6408T26ZD2T
8 - 32Mx8 DDR SDRAM FBGA	PD32M6408T16AD2F
	PD32M6408T26AD2F
	PD32M6408T26ZD2F
16 - 32Mx8 DDR SDRAM TSOP	PD64M6416T16AD2T
	PD64M6416T26AD2T
	PD64M6416T26ZD2T
	PD64M6416T96BD2T
16 - 32Mx8 DDR SDRAM FBGA	PD64M6416T16AD2F
	PD64M6416T26AD2F
	PD64M6416T26ZD2F
	PD64M6416T96BD2F

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	CAS Latency
-5B	**-5B**	**200MHz**	**3**
-6A	**-6A**	**166MHz**	**2.5**
-75A	**-75A**	**133MHz**	**2.5**

GENERAL DESCRIPTION

The modules listed are high performance dynamic random-access 256MB and 512MB modules respectively. These modules are organized in a x64 configuration, and utilize quad bank architecture with a synchronous DDR interface. These DDR SDRAM modules use a double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss .....-1 to +4.6V
Voltage on VddQ Supply relative to Vss……..-1V to +3.6V
Voltage on Vref and Inputs relative to Vss…..-1V to +3.6V
Voltage on I/O pins relative to Vss… -0.5V to VddQ +0.5V
Operating Temperature T_A (Ambient) ..... 25 ° to +70 °C
Storage Temperature ..... -55 to +150 °
Power Dissipation……18 W
Short Circuit Output Current……..50 mA

PIN ASSIGNMENT
184-Pin DIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vref	47	NC	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	NC
3	Vss	49	NC	95	DQ5	141	A10
4	DQ1	50	Vss	96	VddQ	142	NC
5	DQS0	51	NC	97	DQS9	143	VddQ
6	DQ2	52	BA1	98	DQ6	144	NC
7	Vdd	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	VddQ	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	Vdd
11	Vss	57	DQ34	103	NC (A13)	149	DQS13
12	DQ8	58	Vss	104	VddQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	VddQ	61	DQ40	107	DQS10	153	DQ44
16	CK1	62	VddQ	108	Vdd	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	VddQ
19	DQ10	65	CAS#	111	CKE1	157	SO#
20	DQ11	66	Vss	112	VddQ	158	S1#
21	CKE0	67	DQS5	113	NC (BA2)	159	DQS14
22	VddQ	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	NC (A12)	161	DQ46
24	DQ17	70	Vdd	116	Vss	162	DQ47
25	DQS2	71	NC (S2#)	117	DQ21	163	NC(S3#)
26	Vss	72	DQ48	118	A11	164	VddQ
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	Vss	120	Vdd	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	VddQ	76	CK2	122	A8	168	Vdd
31	DQ19	77	VddQ	123	DQ23	169	DQS15
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	VddQ
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	Vddid	128	VddQ	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	Vdd	84	DQ57	130	A3	176	Vss
39	DQ26	85	Vdd	131	DQ30	177	DQS16
40	DQ27	86	DQS7	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	NC	180	VddQ
43	A1	89	Vss	135	NC	181	SA0
44	NC	90	WP	136	VddQ	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	Vdd	92	SCL	138	CKO#	184	VDDSPD

Stresses beyond these may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect reliability.

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Rev: 7/07/05

CAPACITANCE: (This parameter is sampled. Vdd = +2.5V ± 0.2V)

Parameter	Symbol	Max		Units
		256MB	512MB	
Input/Output Capacitance: DQ's, DQS's	C_{I0}	5.0	10.0	pF
Input Capacitance: A0-A12, BA0, BA1, RAS#, CAS#, WE#, S0#	C_{I1}	24.0	48.0	pF
Input Capacitance: S0#, S1#	C_{I2}	24.0	24.0	pF
Input Capacitance: CK0, CK0#	C_{I3}	12.0	15.0	pF
Input Capacitance: CK1, CK1#, CK2, CK2#	C_{I3}	13.5	18.0	pF
Input Capacitance: CKE0 , (CKE1: 512MB only)	C_{I4}	24.0	24.0	pF

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:

Parameter		Symbol	Min	Max	Units
Supply Voltage		Vdd	2.3	2.7	V
I/O Supply Voltage		VddQ	2.3	2.7	V
I/O Reference Voltage		Vref	0.49 x VddQ	0.51 X VddQ	V
I/O Termination Voltage (system)		Vtt	Vref – 0.04	Vref + 0.04	V
Input High (Logic 1) Voltage		$V_{IH(DC)}$	Vref + 0.15	Vdd + 0.3	V
Input Low (Logic 0) Voltage		$V_{IL(DC)}$	-0.3	Vref – 0.15	V
Input Leakage Current Any input = 0V ≤ VIN ≤ Vdd All other pins not under test = 0V	WE#, RAS#, CAS#, BA0, BA1	I_I	-32	32	uA
	S0#, S1#, CKE0, CKE1	I_I	-16	16	uA
	CK0, CK0#	I_I	-8	8	uA
	CK1/CK1#, CK2/CK2#	I_I	-12	12	uA
Output Leakage Current DQs are disabled; 0V ≤ VOUT ≤ VddQ		I_{OZ}	-10	10	uA
Output High Current (V_{OUT} = 1.95V, maximum Vtt)		I_{OH}	-16.8	-	mA
Output Low Current (V_{OUT} = .35V, minimum Vtt)		I_{OL}	16.8	-	mA

AC INPUT OPERATING CONDITIONS: (This parameter is sampled. Vdd = +2.5V ± 0.2V, VddQ = +2.5V ±0.2V)

Parameter	Symbol	MIN	MAX	Units
Input High (Logic 1) Voltage	VIH (AC)	Vref +0.310		V
Input Low (Logic 0) Voltage	VIL (AC)		Vref +0.310	V
I/O Reference Voltage	Vref (AC)	0.49 X VddQ	0.51 x VddQ	V

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IDD OPERATING CONDITIONS AND MAXIMUM LIMITS: Vdd = 2.5V ± .2V, Temp. = 25° to 70 °C

Supply Current		Symbol		-5B	-6A	-75A	Units
OPERATING CURRENT: One bank; Active-Precharge; tRC = tRC MIN; tCK = tCK MIN DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;		Idd0	256MB 512MB	1360 TBD	1080 1160	880	mA mA
OPERATING CURRENT: One bank; Active-read-precharge; Burst = 2; Trc = Trc MIN; CL=2.5; tck = tck MIN; Iout = 0mA; Address and control inputs changing once per clock cycle		Idd1	256MB 512MB	1640 TBD	1160 1240	1000	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; CKE=LOW; tck=tck min		Idd2P	256MB 512MB	80 TBD	80 160	80	mA mA
IDLE STANDBY CURRENT: CS#=HIGH; All banks idle; CKE = HIGH; tck = tck MIN; Address and other control inputs changing once per clock cycle Vin=Vref for DQ, DQS, DM		Idd2F	256MB 512MB	480 TBD	400 800	360	mA mA
ACTIVE POWER DOWN STANDBY CURRENT; One bank Active; power down mode; CKE = low; tck = tck min		Idd3P	256MB 512MB	320 TBD	200 400	160	mA mA
ACTIVE STANDBY CURRENT: CS# = HIGH, CKE = HIGH, One bank Active: trc = tras max; tck = tck min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		Idd3N	256MB 512MB	560 TBD	480 960	440	mA mA
OPERATING CURRENT; Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tck = tck min; Iout = 0mA		Idd4R	256MB 512MB	2200 TBD	1520 1600	920	mA mA
OPERATING CURRENT: Burst =2; Writes; Continuous burst; One bank active; Address and control inputs changing Once per clock cycle; CL=2.5; tck = tck min; DQ, DM and DQS inputs changing twice per clock cycle		Idd4W	256MB 512MB	1480 TBD	1040 1120	960	mA mA
AUTO REFRESH CURRENT	tRC = tRFC MIN	Idd5	256MB 512MB	2240 TBD	2160 4320	2,080	mA mA
OPERATING CURRENT: Four bank interleaving READs (B;=4) with auto precharge, tRC = tRC (MIN); tCK = tRC (MIN); Address and control inputs change only during Active, READ, or WRITE commands.		Idd8	256MB 512MB	3760 TBD	2840 2920	2,680	mA mA

NOTES:

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AC ELECTRICAL CHARACTERISTICS: Vdd = 2.5V ± .2V, Temp. = 25° to 70°C (CL = CAS Latency)

AC CHARACTERISTICS			-5B		-6A		-75A		
PARAMETER		**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
Access window of DQ's from ck/ck#		tAC	-.70	+0.70	-0.70	+0.70	-0.75	0.75	ns
CK high-level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
CK low-level width		tCL			0.45	0.55	0.45	0.55	tCK
Clock cycle time	CL=3 CL=2.5	tCK tCK	5.0	7.5	 6	 12	 7.5	 13	ns
DQ and DM input hold time		tDH	0.40		0.45		0.5		ns
DQ and DM input setup time		tDS	0.40		0.45		0.5		ns
DQ and DM input pulse width (for each input)		tDIPW	1.75		1.75		1.75		ns
Access window of DQS from CK/CK#		tDQSCK	-0.60	+0.60	-0.60	0.60	-0.75	+0.75	ns
DQS input high pulse width		tDQSH	0.35		0.35		0.35		tCK
DQS input low pulse width		tDQSL	0.35		0.35		0.35		tCK
DQS-DQ skew (first to last transition per access)		tDQSQ		0.40		0.45	0.5		ns
Write command to first DQS latching transition		tDQSS	0.72	1.28	0.75	1.25	0.75	1.25	tCK
DQS falling edge to CK rising – setup time		tDSS	0.2		0.2		0.2		tCK
DQS falling edge from CK rising – hold time		tDSH	0.2		0.2		0.2		tCK
Half clock period		tHP	tCH, tCL		tCH, tCL		tCH, tCL		tCK
Data-out high-impedance window from CK/CK#		tHZ		+0.70		0.70		+0.75	ns
Data-out low-impedance window from CK/CK#		tLZ	-0.70		-0.70		-0.75		ns
Address and control input hold time		tIH	0.6		0.75		0.90		ns
Address and control input setup time		tIS	0.6		0.75		0.90		ns
LOAD MODE REGISTER command cycle time		tMRD	10		12		15		ns
Data hold skew factor		tQHS		0.50		0.60		0.75	ns
ACTIVE to PRECHARGE command		tRAS	40	16,000	42	16,000	40	16,000	ns
ACTIVE to READ with auto precharge command		tRAP	NA		NA		NA		ns
ACTIVE to ACTIVE/AUTO REFRESH command period		tRC	55		60		65		ns
AUTO REFRESH command interval		tRFC	70		72		75		us
ACTIVE to READ or WRITE delay		tRCD	15		18		20		ns
PRECHARGE command period		tRP	15		18		20		ns
DQS read preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK
DQS read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
ACTIVE bank a to ACTIVE bank b command		tRRD	10		12		15		ns
DQS Write preamble		tWPRE	0.25		0.25		0.25		tCK
DQS Write preamble setup time		tWPRES	0		0		0		ns
DQS Write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DQS Write recovery time		tWR	15		15		15		ns
Internal WRITE to READ command delay		tWTR	2		1	1			tCK

AC OPERATING CONDITIONS: **(**This parameter is sampled. Vdd = +2.5V ± 0.2V, VddQ = +2.5V ±0.2V)

AC CHARACTERISTICS	Symbol	-5B		-6A		-75A		Units
PARAMETER		**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
ACTIVE bank a to ACTIVE bank b command	tRRD	N/A		12		15		ns
DQS write preamble	tWPRE	0.25		0.25		0.25		tCK
DQS write preamble setup time	tWPRES	0		0		0		ns
DQS write postamble	tWPST	0.4		0.4		0.4	0.6	tCK
Write recovery time	tWR	15		15		15		ns
Internal WRITE to READ command delay	tWTR	2		1		1		tCK
Data valid output window	NA	tQH – tDQSQ						ns
REFRESH to REFRESH command interval	tREFC		70.3		70.3		70.3	us
Average periodic refresh interval	tREFI		15.6		15.6		15.6	us
Terminating voltage delay to Vdd	tVTD	0				0		ns

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SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units
Supply Voltage	V_{CC}	3.0	3.6	V
Input High (Logic 1) Voltage, all inputs	V_{IH}	Vcc x .7	Vcc x .5	V
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	Vcc x .3	V
OUTPUT LOW VOLTAGE, I_{OUT} =3mA	V_{OL}		0.4	V
INPUT LEAKAGE CURRENT, V_{IN} = GND to Vcc	I_{LI}		10	µA
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to Vcc	I_{LO}		10	µA
STANDBY CURRENT SCL=SDA=Vcc -0.3V, All other inputs = GND or 3.3V +10%	I_{SB}		30	µA
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}		2	µA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	µs	
Idle bus time before a transition can start	t_{BUF}	4.7		µs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_{F}		300	ns	
Data-in hold time	$T_{HD:DAT}$	0		µs	
Start condition hold time	$T_{HD:STA}$	4		µs	
Clock HIGH period	t_{HIGH}	4		µs	
Noise suppression time constant at SCL, SDA inputs	t_{I}		100	ns	
Clock LOW period	t_{LOW}	4.7		µs	
SDA and SCL rise time	t_{R}		1	µs	
SCL clock frequency	t_{SCL}		100	KHz	
Data-in setup time	$T_{SU:DAT}$	250		ns	
Start condition setup time	$T_{SU:STA}$	4.7		µs	
Stop condition setup time	$T_{SU:STO}$	4.7		µs	
WRITE cycle time	t_{WR}		10	ms	1

NOTES: 1. The SPD EEPROM WRITE cycle time (t_{WR}) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

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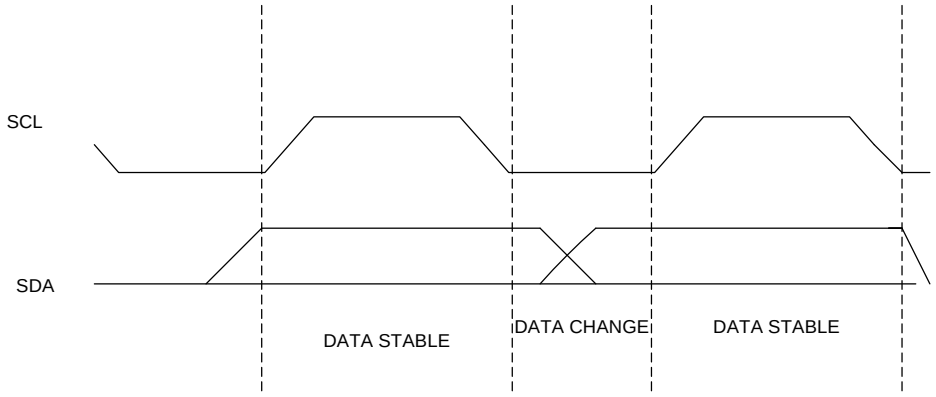

Figure 1
DATA VALIDITY

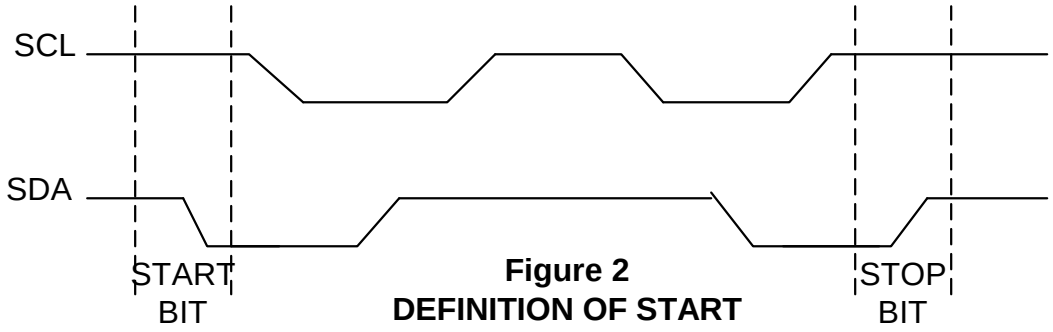

Figure 2
DEFINITION OF START AND STOP

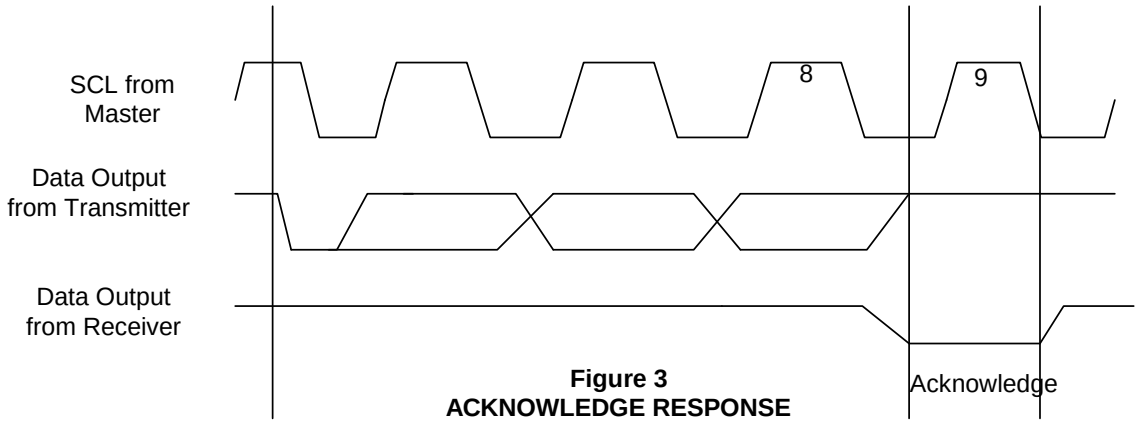

Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

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