



PD64MX6408 (XXX) D2X, PD128MX6416 (XXX) D2X

SDRAM DDR MODULE 64M, 128M X 64 DIMM

Features:

- 184 pin dual in-line memory modules (DIMM)
- Fast data transfer rates PC2700, PC3200
- Utilizes DDR333 and DDR400 DDR SDRAM components
- TSOP or FBGA components.
- 512MB (64MX64), 1GB (128MX64)
- Vdd = 2.5v \pm 0.2v, VddQ = 2.5v \pm 0.2v (-6A & -75A)
- Vdd = 2.6v \pm 0.2v, VddQ = 2.6v \pm 0.2v (-5B)
- 2.5v I/O (SSTL_2 compatible)
- Internal pipelined double data rate (DDR) Architecture, two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/ Received with data
- Differential clock inputs (CK0 and CK0#)
- 7.8125us maximum average periodic refresh interval
- Programmable burst lengths: 2, 4 or 8

Options:

- 8 - 64Mx8 DDR SDRAM TSOP PD64MX6408T27ZD2X
PD64MX6408T37ZD2X
- 8 - 64Mx8 DDR SDRAM FBGA PD64MX6408T27ZD2X
PD64MX6408T37ZD2X
- 16- 64Mx8 DDR SDRAM TSOP PD128MX6416T27ZD2X
PD128MX6416T37ZD2X
- 16- 64Mx8 DDR SDRAM FBGA PD128MX6416T27ZD2X
PD128MX6416T37ZD2X

Part Number:

PIN ASSIGNMENT 184-Pin DIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vref	47	NC	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	NC
3	Vss	49	NC	95	DQ5	141	A10
4	DQ1	50	Vss	96	VddQ	142	NC
5	DQS0	51	NC	97	DQS9	143	VddQ
6	DQ2	52	BA1	98	DQ6	144	NC
7	Vdd	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	VddQ	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	Vdd
11	Vss	57	DQ34	103	NC (A13)	149	DQS13
12	DQ8	58	Vss	104	VddQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	VddQ	61	DQ40	107	DQS10	153	DQ44
16	CK1	62	VddQ	108	Vdd	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	VddQ
19	DQ10	65	CAS#	111	CKE1	157	SO#
20	DQ11	66	Vss	112	VddQ	158	S1#
21	CKE0	67	DQS5	113	NC (BA2)	159	DQS14
22	VddQ	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	NC (A12)	161	DQ46
24	DQ17	70	Vdd	116	Vss	162	DQ47
25	DQS2	71	NC (S2#)	117	DQ21	163	NC(S3#)
26	Vss	72	DQ48	118	A11	164	VddQ
27	A9	73	DQ49	119	DQS11	165	DQ52
28	DQ18	74	Vss	120	Vdd	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	VddQ	76	CK2	122	A8	168	Vdd
31	DQ19	77	VddQ	123	DQ23	169	DQS15
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	VddQ
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	Vddid	128	VddQ	174	DQ60
37	A4	83	DQ56	129	DQS12	175	DQ61
38	Vdd	84	DQ57	130	A3	176	Vss
39	DQ26	85	Vdd	131	DQ30	177	DQS16
40	DQ27	86	DQ57	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	NC	180	VddQ
43	A1	89	Vss	135	NC	181	SA0
44	NC	90	WP	136	VddQ	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	Vdd	92	SCL	138	CK0#	184	VDDSPD

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	CAS Latency
-5B	-5B	200MHz	3
-6A	-6A	166MHz	2.5
-75A	-75A	133MHz	2.5

GENERAL DESCRIPTION

The modules listed are high performance dynamic random-access 512MB and 1GB modules respectively. These modules are organized in a x64 configuration, and utilize quad bank architecture with a synchronous DDR interface. These DDR SDRAM modules use a double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss-1 to +4.6V
 Voltage on VddQ Supply relative to Vss.....-1V to +3.6V
 Voltage on Vref and Inputs relative to Vss.....-1V to +3.6V
 Voltage on I/O pins relative to Vss... -0.5V to VddQ +0.5V
 Operating Temperature T_A (Ambient)25 ° to +70 °C
 Storage Temperature.....-55 to +150 °
 Power Dissipation.....18
 Short Circuit Output Current.....50 mA

Stresses beyond these may cause permanent damage to the device. This is a stress rating only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect reliability.

Spectek Module Part Options and Designations

Options	Designation
Spectek Module	PD
Module Depth & Width	
256MB	32M64
512MB	64M64
1GB	128M64
2 Digit chip count	
8 Chips	08
16 chips	16
Design ID	
Design revision	T26A T26Z T27Z T37Z
Module type	
UDIMM	D
Component type	
X8	2
X16	3
Package Type	
Lead Free FBGA	J
Leaded FBGA	B
Lead Free TSOP	Z
Leaded TSOP	T
Module Speed Grade	
DDR333 PC2700	-6A
DDR400 PC3200	-5B



PD64MX6408 (XXX) D2X, PD128MX6416 (XXX) D2X

CAPACITANCE: 512MB 8 CHIP VERSION (This parameter is sampled. Vdd = +2.5V ± 0.2V)

Parameter	Symbol	512MB		Units
		MIN	MAX	
Input/Output Capacitance: DQ's, DQS's, DM	C ₁₀	4.0	5.0	pF
Input Capacitance: Command and Address, S#, CKE	C ₁₁	16.0	24.0	pF
Input Capacitance: CK0, CK0#	C ₁₂	10.0	12.0	pF
Input Capacitance: CK1, CK1#, CK2, CK2#	C ₁₃	9.0	12.0	pF
Input Capacitance: SDA	C ₁₃	-	8.0	pF
Input Capacitance: SCL, SA0, SA2	C ₁₄	-	6.0	pF

CAPACITANCE: 1GB 16 CHIP VERSION (This parameter is sampled. Vdd = +2.5V ± 0.2V)

Parameter	Symbol	1GB		Units
		MIN	MAX	
Input/Output Capacitance: DQ's, DQS's, DM	C ₁₀	8.0	10.0	pF
Input Capacitance: Command and Address	C ₁₁	32.0	48.0	pF
Input Capacitance: S#, CKE	C ₁₁	16.0	24.0	pF
Input Capacitance: CK0, CK0#	C ₁₂	11.0	15.0	pF
Input Capacitance: CK1, CK1#, CK2, CK2#	C ₁₃	12.0	18.0	pF
Input Capacitance: SDA	C ₁₃	-	8.0	pF
Input Capacitance: SCL, SA0, SA2	C ₁₄	-	6.0	pF

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS:

Parameter	Symbol	Min	Max	Units	
Supply Voltage (For -6A and -75A)	Vdd	2.3	2.7	V	
I/O Supply Voltage (For -6A and -75A)	VddQ	2.3	2.7	V	
Supply Voltage (For -5B)	Vdd	2.5	2.7	V	
I/O Supply Voltage (For -5B)	VddQ	2.5	2.7	V	
I/O Reference Voltage	Vref	0.49 x VddQ	0.51 X VddQ	V	
I/O Termination Voltage (system)	Vtt	Vref - 0.04	Vref + 0.04	V	
Input High (Logic 1) Voltage	V _{IH(DC)}	Vref + 0.15	Vdd + 0.3	V	
Input Low (Logic 0) Voltage	V _{IL(DC)}	-0.3	Vref - 0.15	V	
Input Leakage Current Any input = 0V ≤ VIN ≤ Vdd All other pins not under test = 0V	WE#, RAS#, CAS#, BA0, BA1	I _I	-32	32	uA
	S0#, S1#, CKE0, CKE1	I _I	-16	16	uA
	CK0, CK0#	I _I	-8	8	uA
	CK1/CK1#, CK2/CK2#	I _I	-12	12	uA
Output Leakage Current DQs are disabled; 0V ≤ VOUT ≤ VddQ	I _{OZ}	-10	10	uA	
Output High Current (V _{OUT} = 1.95V, maximum Vtt)	I _{OH}	-16.8	-	mA	
Output Low Current (V _{OUT} = .35V, minimum Vtt)	I _{OL}	16.8	-	mA	

AC INPUT OPERATING CONDITIONS: (This parameter is sampled. Vdd = +2.5V ± 0.2V, VddQ = +2.5V ± 0.2V)

Parameter	Symbol	MIN	MAX	Units
Input High (Logic 1) Voltage	V _{IH} (AC)	Vref + 0.310		V
Input Low (Logic 0) Voltage	V _{IL} (AC)		Vref + 0.310	V
I/O Reference Voltage	Vref (AC)	0.49 X VddQ	0.51 x VddQ	V



PD64MX6408 (XXX) D2X, PD128MX6416 (XXX) D2X

IDD OPERATING CONDITIONS AND MAXIMUM LIMITS: Vdd = 2.5V ± .2V, Temp. = 25° to 70 °C

Supply Current		Symbol		-5B	-6A	-75A	Units
OPERATING CURRENT: One bank; Active-Precharge; tRC = tRC MIN; tCK = tCK MIN DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles;		Idd0	512MB 1GB	1240 TBD	1080 TBD	960	mA mA
OPERATING CURRENT: One bank; Active-read-precharge; Burst = 2; Trc = Trc MIN; CL=2.5; tck = tck MIN; Iout = 0mA; Address and control inputs changing once per clock cycle		Idd1	512MB 1GB	1480 TBD	1280 TBD	1080	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; CKE=LOW; tck=tck min		Idd2P	512MB 1GB	80 TBD	80 TBD	80	mA mA
IDLE STANDBY CURRENT: CS#=HIGH; All banks idle; CKE = HIGH; tck = tck MIN; Address and other control inputs changing once per clock cycle Vin=Vref for DQ, DQS, DM		Idd2F	512MB 1GB	440 TBD	400 TBD	400	mA mA
ACTIVE POWER DOWN STANDBY CURRENT; One bank Active; power down mode; CKE = low; tck = tck min		Idd3P	512MB 1GB	360 TBD	280 TBD	200	mA mA
ACTIVE STANDBY CURRENT: CS# = HIGH, CKE = HIGH, One bank Active: trc = tras max; tck = tck min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle		Idd3N	512MB 1GB	480 TBD	440 TBD	440	mA mA
OPERATING CURRENT; Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 2.5; tck = tck min; Iout = 0mA		Idd4R	512MB 1GB	1520 TBD	1360 TBD	1240	mA mA
OPERATING CURRENT: Burst =2; Writes; Continuous burst; One bank active; Address and control inputs changing Once per clock cycle; CL=2.5; tck = tck min; DQ, DM and DQS inputs changing twice per clock cycle		Idd4W	512MB 1GB	1520 TBD	1240 TBD	1040	mA mA
AUTO REFRESH CURRENT	tRC = tRFC MIN	Idd5	512MB 1GB	2760 TBD	2080 TBD	2080	mA mA
OPERATING CURRENT: Four bank interleaving READs (B;=4) with auto precharge, tRC = tRC (MIN); tCK = tRC (MIN); Address and control inputs change only during Active, READ, or WRITE commands.		Idd7	512MB 1GB	3600 TBD	3200 TBD	2680	mA mA

NOTES:



PD64MX6408 (XXX) D2X, PD128MX6416 (XXX) D2X

AC ELECTRICAL CHARACTERISTICS: Vdd = 2.5V ± .2V, Temp. = 25° to 70°C (CL = CAS Latency)

AC CHARACTERISTICS			-5B		-6A		-75A		
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	
Access window of DQ's from ck/ck#	tAC	-0.70	+0.70	-0.70	+0.70	-0.75	0.75	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL			0.45	0.55	0.45	0.55	tCK	
Clock cycle time	CL=3	tCK	5.0	7.5	6	13	7.5	13	ns
	CL=2.5	tCK							
DQ and DM input hold time	tDH	0.40		0.45		0.5		ns	
DQ and DM input setup time	tDS	0.40		0.45		0.5		ns	
DQ and DM input pulse width (for each input)	tDIPW	1.75		1.75		1.75		ns	
Access window of DQS from CK/CK#	tDQSCK	-0.60	+0.60	-0.60	0.60	-0.75	+0.75	ns	
DQS input high pulse width	tDQSH	0.35		0.35		0.35		tCK	
DQS input low pulse width	tDQSL	0.35		0.35		0.35		tCK	
DQS-DQ skew (first to last transition per access)	tDQSQ		0.40		0.45		0.5	ns	
Write command to first DQS latching transition	tDQSS	0.72	1.28	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK rising – setup time	tDSS	0.2		0.2		0.2		tCK	
DQS falling edge from CK rising – hold time	tDSH	0.2		0.2		0.2		tCK	
Half clock period	tHP	tCH, tCL		tCH, tCL		tCH, tCL		tCK	
Data-out high-impedance window from CK/CK#	tHZ		+0.70		0.70		+0.75	ns	
Data-out low-impedance window from CK/CK#	tLZ	-0.70		-0.70		-0.75		ns	
Address and control input hold time (fast slew rate)	tIHF	0.6		0.75		0.90		ns	
Address and control input setup time (fast slew rate)	tISF	0.6		0.75		0.90		ns	
Address and control input hold time (slow slew rate)	tIHS	0.7		0.80		1.00		ns	
Address and control input setup time (slow slew rate)	tISS	0.7		0.80		1.00		ns	
LOAD MODE REGISTER command cycle time	tMRD	10		12		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	tQH	thp- tqhs		thp- tqhs		thp- tqhs			
Data hold skew factor	tQHS		0.50		0.60		0.75	ns	
ACTIVE to PRECHARGE command	tRAS	40	70,000	42	70,000	45	70,000	ns	
ACTIVE to READ with auto precharge command	tRAP	NA		NA		NA		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	tRC	55		60		65		ns	
AUTO REFRESH command period	tRFC	70		72		75		us	
ACTIVE to READ or WRITE delay	tRCD	15		18		20		ns	
PRECHARGE command period	tRP	15		18		20		ns	
DQS read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
DQS read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
ACTIVE bank a to ACTIVE bank b command	tRRD	10		12		15		ns	
DQS Write preamble	tWPRE	0.25		0.25		0.25		tCK	
DQS Write preamble setup time	tWPRES	0		0		0		ns	
DQS Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS Write recovery time	tWR	15		15		15		ns	
Internal WRITE to READ command delay	tWTR	2		1		1		tCK	

AC OPERATING CONDITIONS: (This parameter is sampled. Vdd = +2.5V ± 0.2V, VddQ = +2.5V ± 0.2V)

AC CHARACTERISTICS	Symbol	-5B		-6A		-75A		Units
PARAMETER		MIN	MAX	MIN	MAX	MIN	MAX	
Data valid output window	NA	tQH – tDQSQ						ns
REFRESH to REFRESH command interval	tREFC		70.3		70.3		70.3	us
Average periodic refresh interval	tREFI		7.81		7.81		7.81	us
Terminating voltage delay to Vdd	tVTD	0				0		ns



PD64MX6408 (XXX) D2X, PD128MX6416 (XXX) D2X

SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

PARAMETER/CONDITION	Symbol	MIN	MAX	Units
Supply Voltage	V _{CC}	3.0	3.6	V
Input High (Logic 1) Voltage, all inputs	V _{IH}	V _{CC} x .7	V _{CC} x .5	V
Input Low (Logic 0) Voltage, all inputs	V _{IL}	-1.0	V _{CC} x .3	V
OUTPUT LOW VOLTAGE, I _{OUT} = 3mA	V _{OL}		0.4	V
INPUT LEAKAGE CURRENT, V _{IN} = GND to V _{CC}	I _{LI}		10	μA
OUTPUT LEAKAGE CURRENT, V _{OUT} = GND to V _{CC}	I _{LO}		10	μA
STANDBY CURRENT SCL=SDA=V _{CC} -0.3V, All other inputs = GND or 3.3V +10%	I _{SB}		30	μA
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I _{CC}		2	μA

SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS (VCC = +3.3V ± 0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	Symbol	MIN	MAX	Units	Notes
SCL LOW to SDA data-out valid	¹ AA	0.3	3.5	μs	
Idle bus time before a transition can start	¹ BUF	4.7		μs	
Data-out hold time	¹ DH	300		ns	
SDA and SCL fall time	¹ F		300	ns	
Data-in hold time	¹ HD:DAT	0		μs	
Start condition hold time	¹ HD:STA	4		μs	
Clock HIGH period	¹ HIGH	4		μs	
Noise suppression time constant at SCL, SDA inputs	¹ I		100	ns	
Clock LOW period	¹ LOW	4.7		μs	
SDA and SCL rise time	¹ R		1	μs	
SCL clock frequency	¹ SCL		100	KHz	
Data-in setup time	¹ SU:DAT	250		ns	
Start condition setup time	¹ SU:STA	4.7		μs	
Stop condition setup time	¹ SU:STO	4.7		μs	
WRITE cycle time	¹ WR		10	ms	1

NOTES: 1. The SPD EEPROM WRITE cycle time (¹WR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

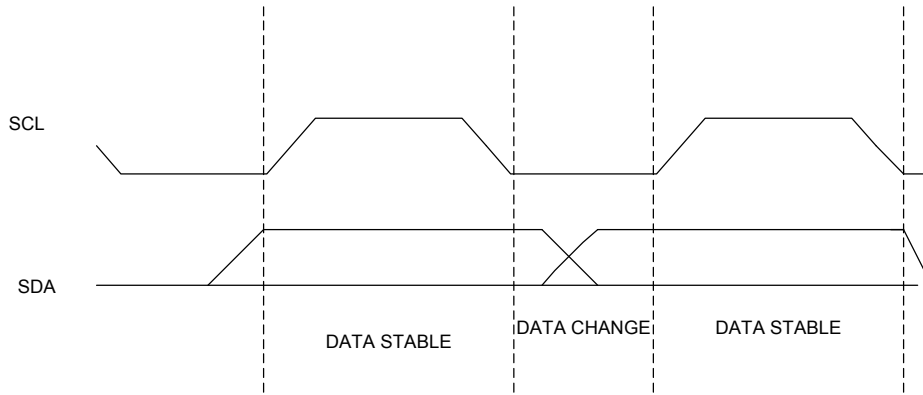


Figure 1
DATA VALIDITY

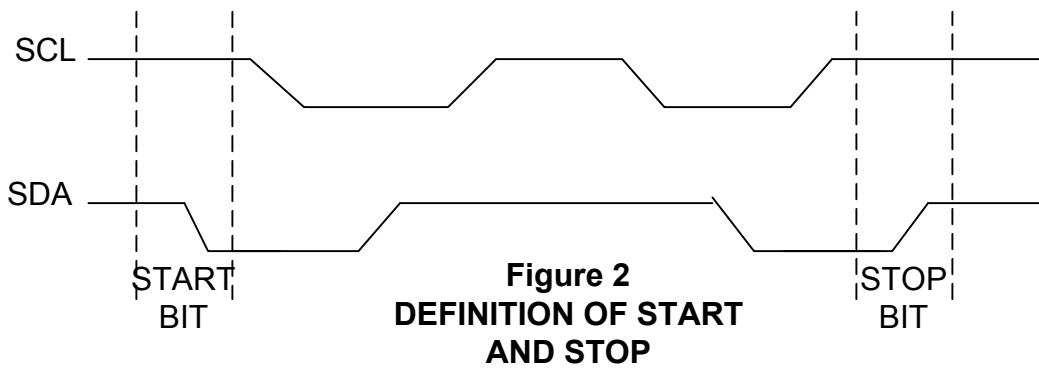


Figure 2
DEFINITION OF START
AND STOP

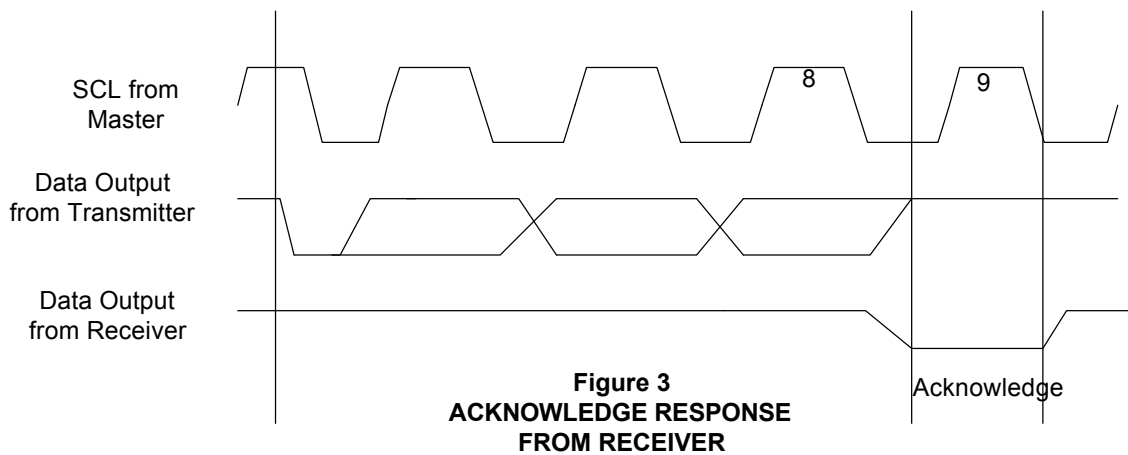


Figure 3
ACKNOWLEDGE RESPONSE
FROM RECEIVER