DDR3 SDRAM

PRA512M8V70SG8RAF-15E

PRA 512M8 – 64 Meg x 8 x 8 Banks

Features

- Vdd = VddQ = 1.5V ±0.075V
- 1.5V center-terminated push / pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) For data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS]
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- Tc of 0C to +95C
  - 64ms 8192 cycle refresh at 0C to 85C
  - 32ms 8192 cycle refresh at +85C to +95C
- Self refresh temperature (SRT)
- Write leveling
- Multipurposes register
- Output driver calibration

Options	**Marking**
SpecTek Component	PRA
Configuration	
-512MX8	512M8
Product Code	
-DDR3	Vx
Density	
4Gb	0x
Voltage/ Refresh	
1.5V/8K Refresh	GD
FBGA package (Pb-free) - x4, x8	
- 78-ball (10.5mm x 12mm) Rev. D	RAF
- 78-ball (9mm x 10.5mm) Rev. E	RHF
FBGA package (Pb-free) - x16	
- 96-ball (10mm x 14mm) Rev. D	REF
- 96-ball (9mm x 14mm) Rev. E	HAF
Timing - cycle time	
- 1.07ns @ CL = 13 (DDR3-1866)	-107
- 1.25ns @ CL = 11 (DDR3-1600)	-125
- 1.5ns @ CL = 9 (DDR3-1333)	-15E
- 1.87ns @ CL = 7 (DDR3-1066)	-187E

Note: Contact Spectek sales for details on product availability

COMPONENT MARKING and TIMING PARAMETERS

Speed Marking	Component Marking	Clock Frequency	CAS Latency
-15E	**PEB04 -15E**	**800MHz**	**9**

GENERAL DESCRIPTION

The PRA512M8V70SG8RAF-15E is high performance dynamic random-access 4Gb device respectively. These components are organized in a x8 configuration, and utilize 8 bank architecture with a synchronous DDR3 interface. These DDR3 SDRAM components use double data rate architecture to achieve high speed operation.

The PRA components are restricted to 8 chip module assemblies only and are only approved for use on standard UDIMM module assemblies.

ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss .....-0.4V to 1.975V
Voltage on Vdd Supply relative to VssQ…..-0.4V to1.975V
Voltage on any pin relative to Vss……..-0.4V to1.975V
Operating Temperature T_A (Ambient) ..... 0 ° to 95 °C
Storage Temperature ..... -55 to +150 °C

Stresses beyond the above listed parameters may cause permenent damage to the device. This is a stress only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect device reliability.

Addressing

Parameter	1 Gig × 4	512 Meg × 8	256 Meg × 16
Configuration	128 Meg x 4 x 8 banks	64 Meg x 8 x 8 banks	32 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	64K (A[15:0])	64K (A[15:0])	32K (A[14:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

Spectek Part Number Matrix

PRA512M8V70SG8RAF-15E

PRA: Spectek Branded Approved for 8 chip assemblies only
Component Depth: 512Mb
Component Width: x8
Design ID: V70S
Operating Voltage: G: 1.5V
Refresh rate: 8: 8K
Component package: 78-ball (10.5mm x 12mm) Rev. D RAF
Material type: F: Lead-free
Speed grade: -15E: PC3-10600 DDR3-1333

FBGA Part Marking

PRA: PEB04 -15E

Functional Description

The DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

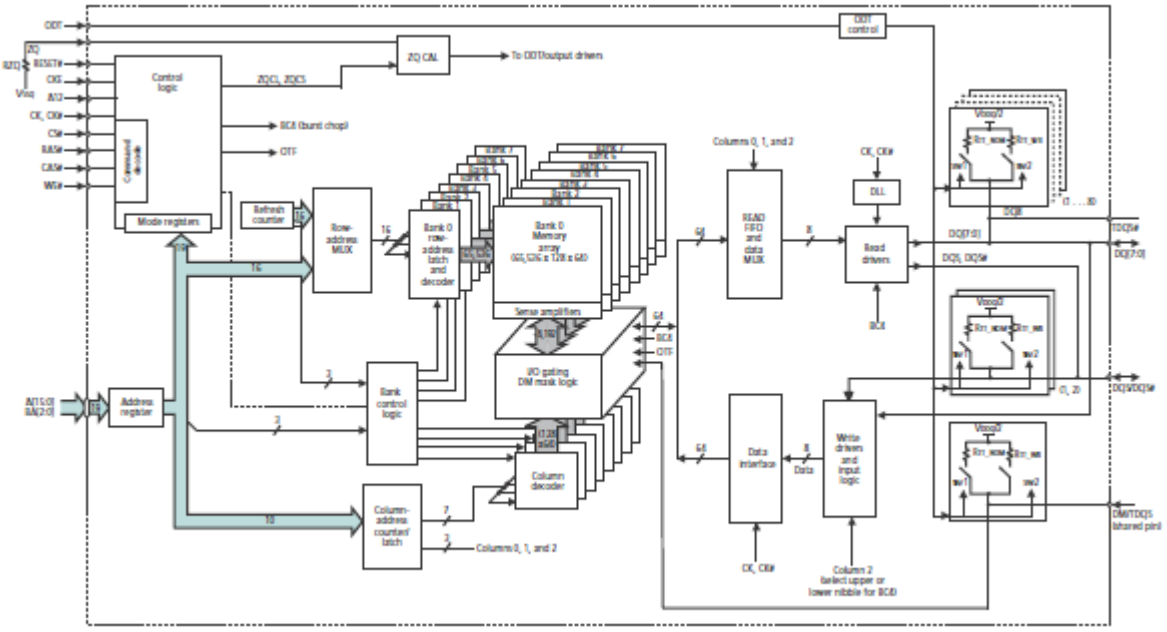
Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM use READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

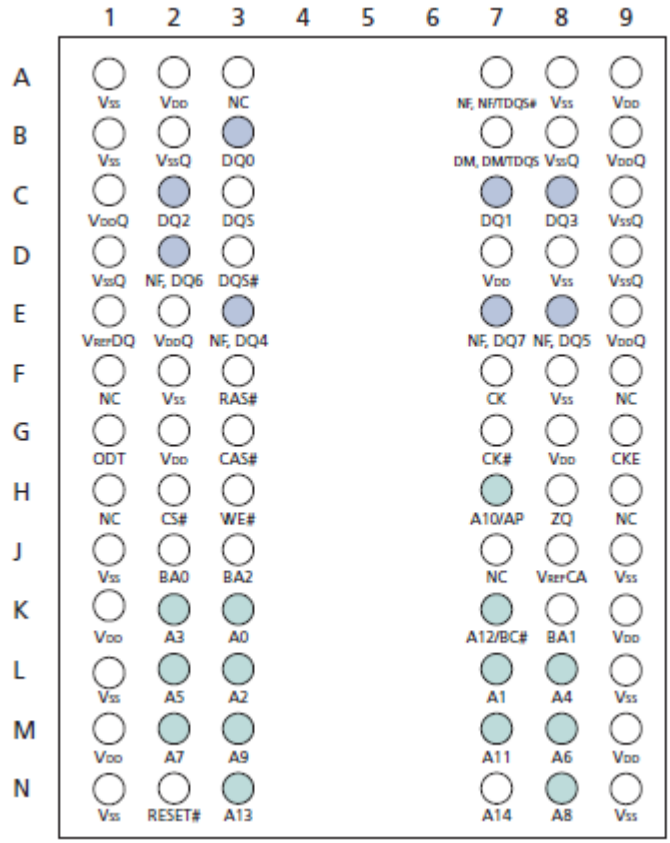
As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Functional Block Diagram



Ball Assignments and Descriptions
78 Ball FBGA X8 (Top view)



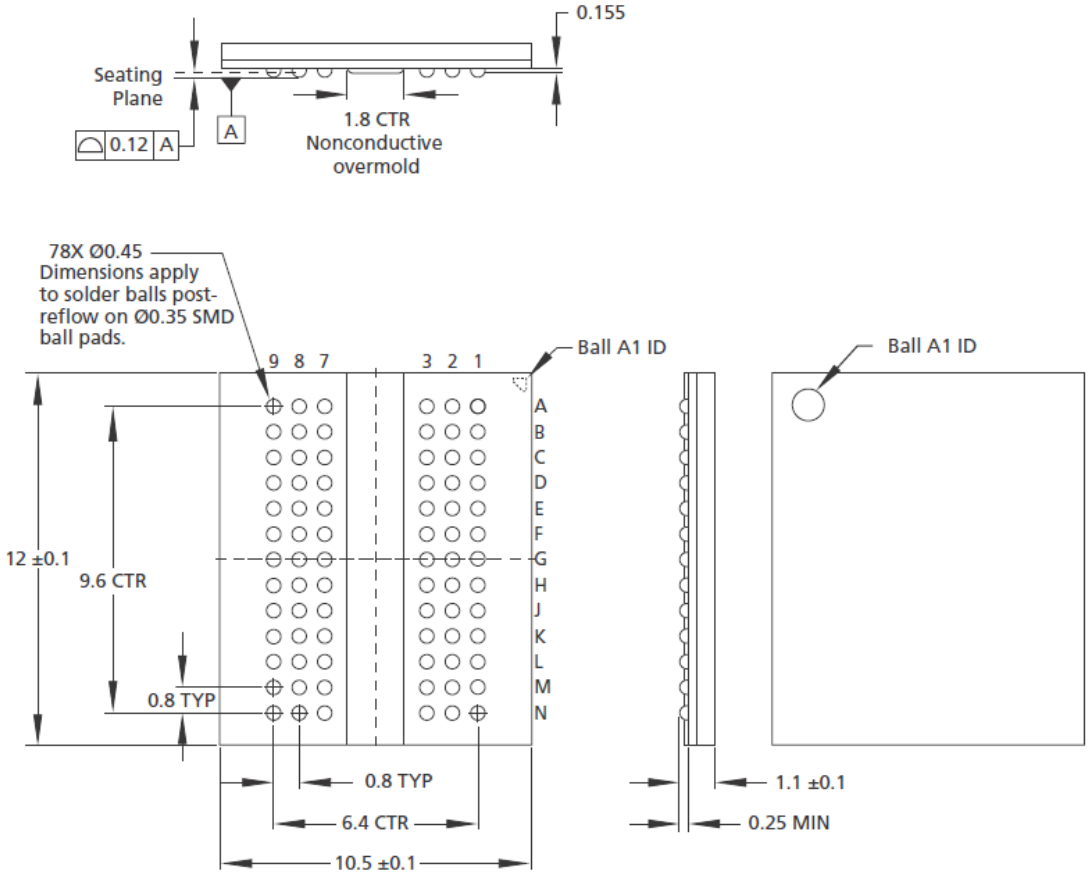
Ball Descriptions

Symbol	Type	Description
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10/AP, A11, A12/BC#, A13, A14	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VREFCA. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4 burst chop).
BA0, BA1, BA2	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VREFCA.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during power-down. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to VREFCA.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to VREFCA.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input data during a write access. Although the DM ball is input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to VREFDQ. DM has an optional use as TDQS on the x8.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[7:0], DQS, DQS#, and DM for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to VREFCA.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to VREFCA.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × VDD and DC LOW ≤ 0.2 × VDDQ. RESET# assertion and desertion are asynchronous.
DQ0, DQ1, DQ2, DQ3	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to VREFDQ.
DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, DQ7	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to VREFDQ.
DQS, DQS#	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	Output	**Termination data strobe:** Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.

Ball Descriptions Continued

Symbol	Type	Description
VDD	Supply	**Power supply:** 1.5V ±0.075V.
VDDQ	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
VREFCA	Supply	**Reference voltage for control, command, and address:** VREFCA must be maintained at all times (including self refresh) for proper device operation.
VREFDQ	Supply	**Reference voltage for data:** VREFDQ must be maintained at all times (excluding self refresh) for proper device operation.
VSS	Supply	Ground.
VSSQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to VSSQ.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	**No function:** When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

PRA512M8V70SG8RAF-15E
78-ball (10.5mm x 12mm) Rev. D RAF



Notes: 1. All dimensions are in millimeters.