SPECTEK®

PRN256M16V00HG8GNF-125

DDR3 SDRAM
PRN256M16V00HG8GNF-125

PRN 256M16 – 32 Meg x 16 x 8 Banks

Features

- Vdd = VddQ = 1.5V ±0.075V
- 1.5V center-terminated push / pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) For data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS]
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- Tc of 0C to +95C
  - 64ms 8192 cycle refresh at 0C to 85C
  - 32ms 8192 cycle refresh at +85C to +95C
- Self refresh temperature (SRT)
- Write leveling
- Multipurposes register
- Output driver calibration

Options	Marking
SpecTek Component	PRN
Configuration -256x16	256M16
Product Code -DDR3	Vx
Density 4Gb	0x
Voltage/ Refresh 1.5V/8K Refresh	G8
FBGA package (Pb-free) – X16 -96-ball (8mmx14mm) rev E	GNF
Timing – cycle time 1.25ns @ CL = 11 (DDR3-1600)	-125

Note: Contact Spectek sales for details on product availability

COMPONENT MARKING and TIMING PARAMETERS

Speed Marking	Component Marking	Clock Frequency	CAS Latency
-125	PE029 -125	800MHz	11

GENERAL DESCRIPTION

The PRN256M16V00HG8GNF-125 is a high performance dynamic random-access 4Gb device. These components are organized in a x16 configuration, and utilize 8 bank architecture with a synchronous DDR3 interface. These DDR3 SDRAM components use double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss....... -0.4V to 1.975V
Voltage on Vdd Supply relative to VssQ…..-0.4V to1.975V
Voltage on any pin relative to Vss…………..-0.4V to1.975V
Operating Temperature T_A (Ambient) .... 0 ° to 95 °C
Storage Temperature ....-55 to +150 °C

Stresses beyond the above listed parameters may cause permenent damage to the device. This is a stress only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect device reliability.

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Addressing

Parameter	1 Gig × 4	512 Meg × 8	256 Meg × 16
Configuration	128 Meg x 4 x 8 banks	64 Meg x 8 x 8 banks	32 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	64K (A[15:0])	64K (A[15:0])	32K (A[14:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

Spectek Part Number Matrix

PRN256M16V00HG8GNF-125

PRN: Spectek Branded Device
Component Depth: 256Mb
Component Width: x16
Design ID: V00H
Operating Voltage: G: 1.5V
Refresh rate: 8: 8K
Component package: 96-ball (8 x 14MM) GNF
Material type: F: Lead-free
Speed grade: -125: PC3-12800 DDR3-1600

FBGA Part Marking

PRN: PE 029 -125

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Functional Description

The DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM use READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

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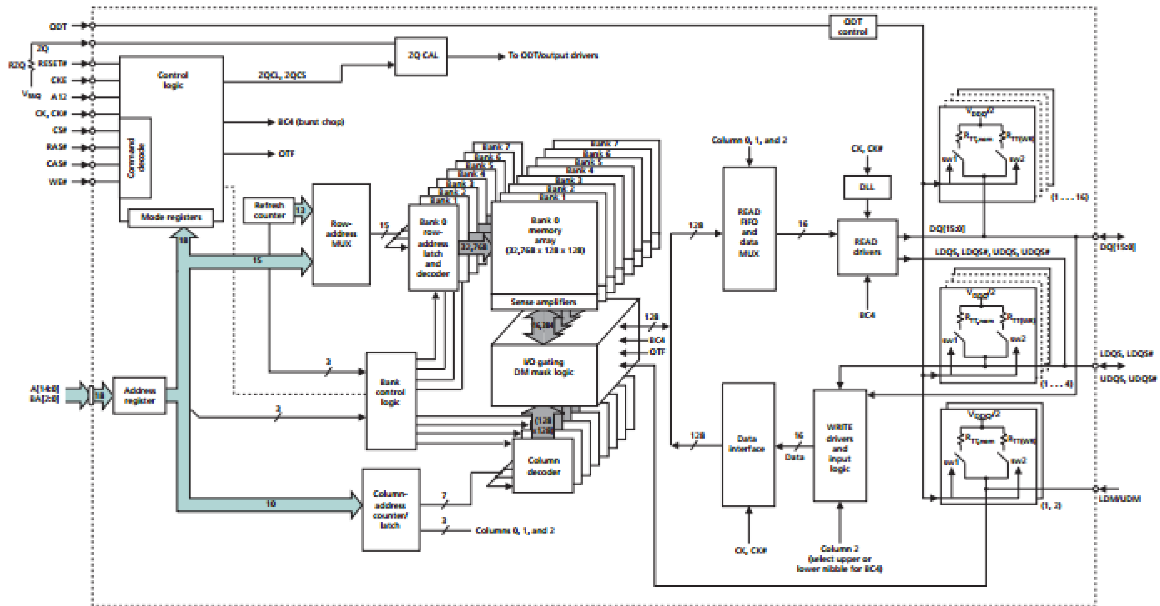
256 Meg x 16 Functional Block Diagram



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Ball Assignments and Descriptions
96 Ball FBGA X16 (Top view)

	1	2	3	4	5	6	7	8	9
A	V_{DDQ}	DQ13	DQ15				DQ12	V_{DDQ}	V_{SS}
B	V_{SSQ}	V_{DD}	V_{SS}				UDQS#	DQ14	V_{SSQ}
C	V_{DDQ}	DQ11	DQ9				UDQS	DQ10	V_{DDQ}
D	V_{SSQ}	V_{DDQ}	UDM				DQ8	V_{SSQ}	V_{DD}
E	V_{SS}	V_{SSQ}	DQ0				LDM	V_{SSQ}	V_{DDQ}
F	V_{DDQ}	DQ2	LDQS				DQ1	DQ3	V_{SSQ}
G	V_{SSQ}	DQ6	LDQS#				V_{DD}	V_{SS}	V_{SSQ}
H	V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}
J	NC	V_{SS}	RAS#				CK	V_{SS}	NC
K	ODT	V_{DD}	CAS#				CK#	V_{DD}	CKE
L	NC	CS#	WE#				A10/AP	ZQ	NC
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}
N	V_{DD}	A3	A0				A12/BC#	BA1	V_{DD}
P	V_{SS}	A5	A2				A1	A4	V_{SS}
R	V_{DD}	A7	A9				A11	A6	V_{DD}
T	V_{SS}	RESET#	A13				A14	A8	V_{SS}

Notes:
1. Ball descriptions listed in Table 4 (page 20) are listed as “x4, x8” if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

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96b X16 Ball Descriptions

Symbol	Type	Description
A[14:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See Table 70 (page 116).
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.

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Ball Descriptions Continued

Symbol	Type	Description
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.5V ±0.075V.
V_{DDQ}	Supply	**DQ power supply:** 1.5V ±0.075V. Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

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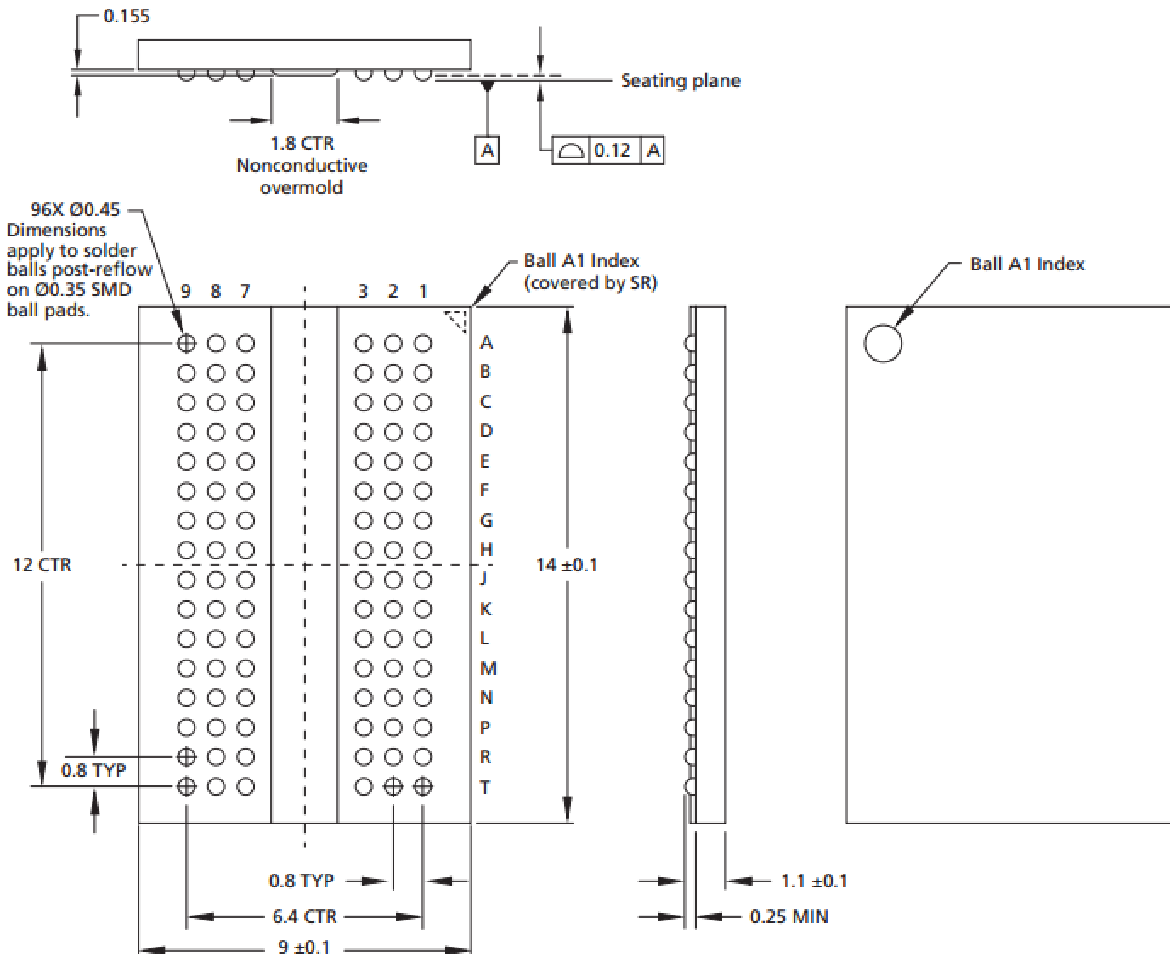
PRN256M16V00HG8GNF-125

96-ball (8mm x 14mm) GNF



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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