SDRAM DDR3 512MX8 ½ Density Device Technical Note

Introduction

This technical note provides an overview of how the PRN256M8V70SG8RAF-15E DDR3 SDRAM device is configured and tested as a 2Gb device.
This deivce is internaly configured as a standard 2Gb 256MX8 JEDEC standard device.

Addressing

Parameter	4Gb ½ Density Device Configuration 2Gb 256M X8	4Gb Device Configuration for reference only 4Gb 512M X 8
Configuration	32MEG X 8 X 8 Banks	64MEG X 8 X 8 Banks
Refresh count	8K	8K
Row addressing	32K A0-A14	64K A0-A15
Bank addressing	8: BA0-BA2	8: BAO-BA2
Column addressing	1K A0-A9	1K A0-A9
Page Size	1KB	1KB

Spectek Component Part Options and Designations

Options	Designation
Spectek Memory	**PRN Spectek Component sales (Approved for 8 chip assemblies)**
Component depth	**256MEG**
Component width	**x8**
Design ID	**V70S (1/2 density device)**
Operating voltage	**1.5V**
Refresh	**8: 8K**
Component package type:	**RA: 78/117B 10.5X12MM**
Material type	**F: LEAD-FREE**
Device speed	**-15E 1333MHz 9-9-9-1.5V**

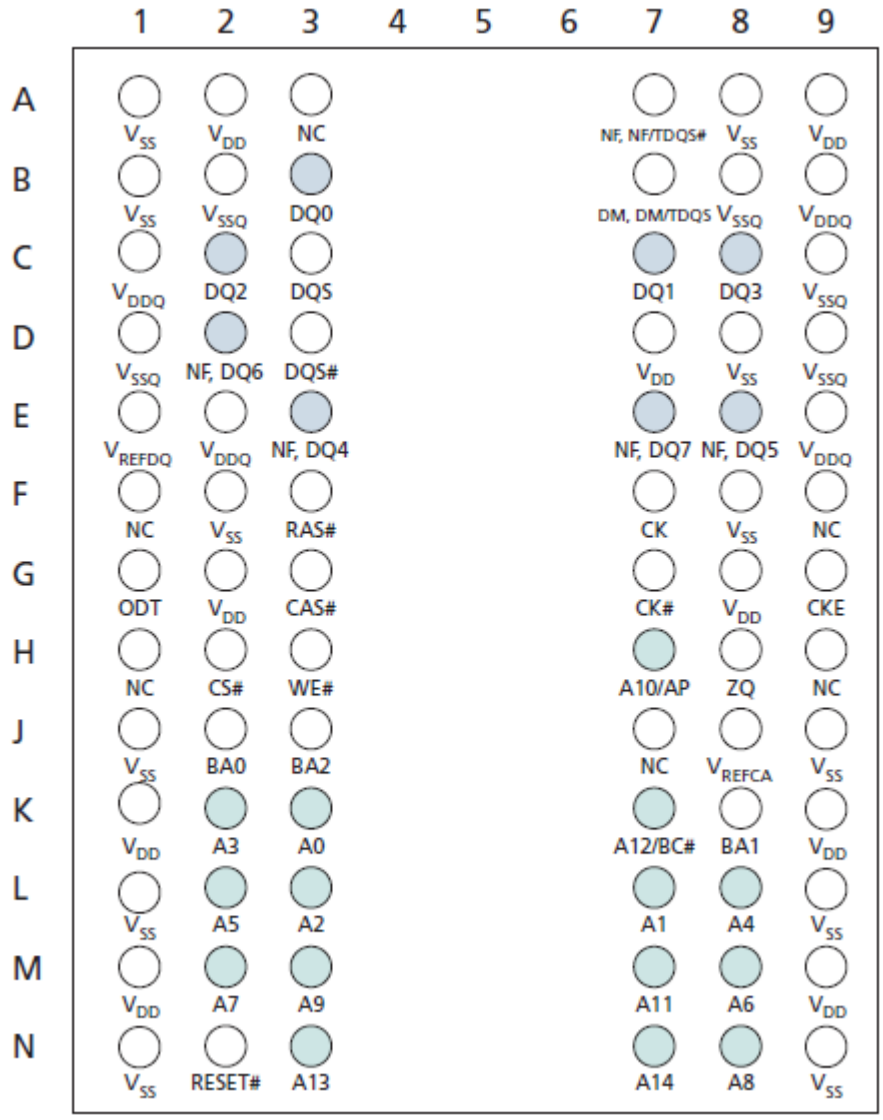
Pin Descriptions

Symbol	Type	Description
A0-A14	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to Vrefca. A12: When enable in the mode register (MR), A12 is sampled during READ adn WRTIE commands to determne whether burst chop (on-the-fly) will be perfrmed (HIGH = BL8 or no burst chop, LOW = BC4)
BA0-BA2	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MRO, MR1, MR2 or MR3) is loaded during the LOAD MODE command.BA[2:0] are reference to Vrefca
CKx CKx#	Input	**Clock:** Differential clock inputs. All control command and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS,DSS#) is referenced to crossings of CK and CK#.
CKE	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
DM	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODT	Input	**On-die termination:** Enables (registered HIGH) and disables (register LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS. DQS#, DM and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS# and WE# (along with CS#) define the command being entered.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to rail signal wiht DC HIGH $\geq$0.8 x Vdd and DC LOW $\leq$ 0.2X Vddq. RESET# asserion and deseerion are asynchronous.
DQ0- DQ7	I/O	**Data input/output:** Bidirectional data bus.
DQS DQS#	I/O	**Data strobe:** Differential data strobes. Output with read data: edge-aligned with read data: input with read data: input with write data: center-aligned with write data

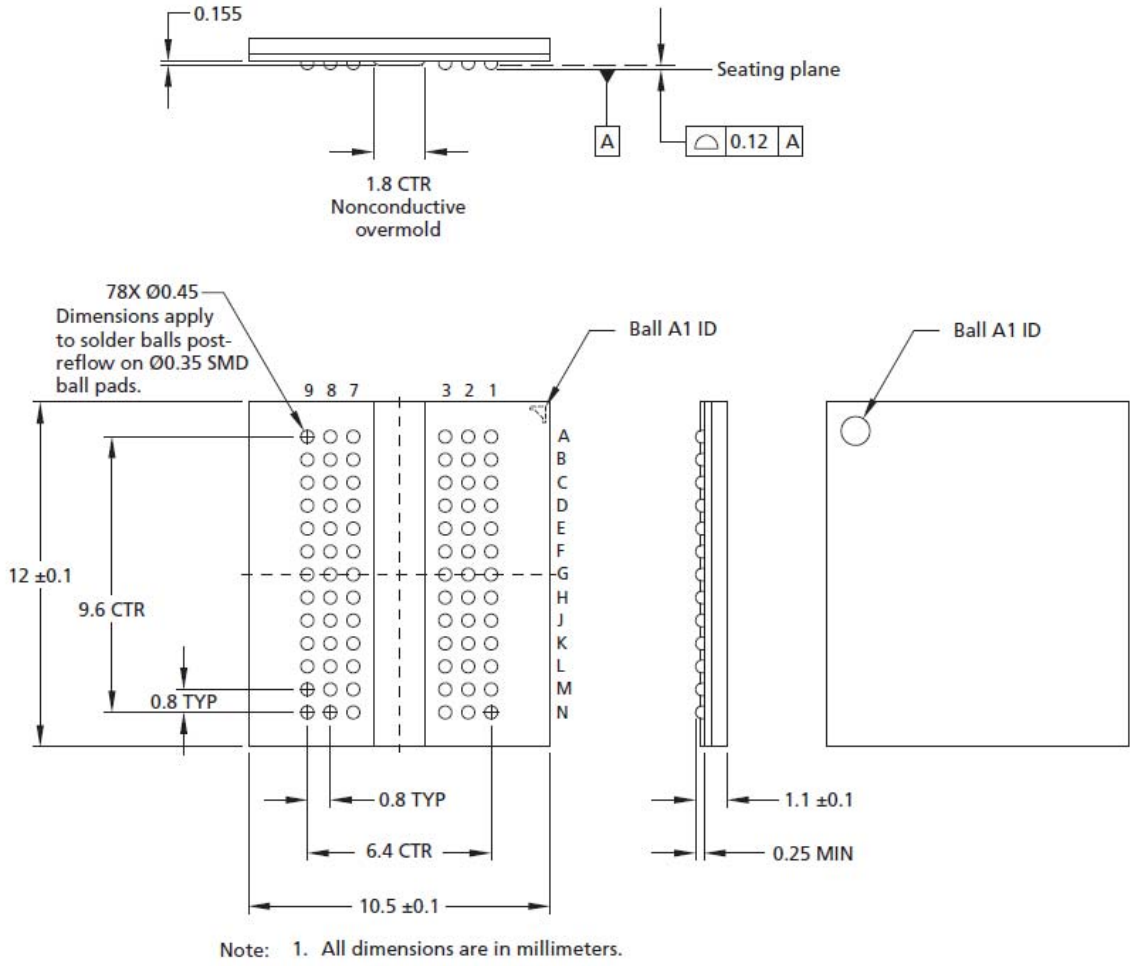
Pin Descriptions - Continued)

Symbol	Type	Description
TDQS TDQSx#	Output	**Termination data strobe (x8 devices only)** When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance:.
Vdd	Supply	**Power Supply:** 1.5V ±0.1V.
VddQ	Supply	**DQ Power Supply:** 1.5V ±0.1V Isolated on the device for improved noise immunity.
Vddrefca	Supply	**Reference voltage for control, command and address:** Vrefca must be maintained at all times (including self refresh) for proper device operation.
Vrefdq	Supply	**Reference voltage for data:** Vrefdq must be maintained at all times (excluding self refresh) for proper device operation.
Vss	Supply	Ground
VssQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240 ohm resistor (RZQ) which is tied to Vssq.
NC	-	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls)
NF	-	**No function:** When configured as X4 device, these balls are NF. When configured as X8 device, these balls are defined as TDQS#,DQ[7:4].

Ball Assignments and Descriptions
78 – Ball FBGA X8 (Top View)



78 – Ball FBGA Package 10.5MM X 12 MM (RA x8 Package)



Note: 1. All dimensions are in millimeters.

