

# DDR3 SDRAM

## PRN256M8V79BG8GQF-15E

PRN 256M8 – 32 Meg x 8 x 8 Banks

### Features

- Vdd = VddQ = 1.5V ±0.075V
- 1.5V center-terminated push / pull I/O
- Differential bidirectional data strobe
- 8n-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) For data, strobe, and mask signals
- Programmable CAS READ latency (CL)
- Posted CAS additive latency (AL)
- Programmable CAS WRITE latency (CWL) based on tCK
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- Tc of 0C to +95C
  - 64ms 8192 cycle refresh at 0C to 85C
  - 32ms 8192 cycle refresh at +85C to +95C
- Self refresh temperature (SRT)
- Write leveling
- Multipurposes register
- Output driver calibration

### Options

SpecTek Component

### Marking

PRN

Configuration -256MX8	256M8
Product Code -DDR3	Vx
Density 2Gb	8x
Voltage/ Refresh 1.5V/8K Refresh	G8
FBGA Package (PB-free) x8 78/117B 8 x 10.5MM	GQF
FBGA Package (Leaded) 78/117B 8 x 10.5MM	GQL
Timing – cycle time 1.5ns @ CL 9 (DDR3 – 1333)	-15E

Note: Contact Spectek sales for details on product availability

### COMPONENT MARKING and TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	CAS Latency
-15E	PE903-15E	667MHz	9

### GENERAL DESCRIPTION

The PRN256M8V79BG8GQF-15E is high performance dynamic random-access 2Gb device respectively. These components are organized in a x8 configuration, and utilize 8 bank architecture with a synchronous DDR3 interface. These DDR3 SDRAM components use double data rate architecture to achieve high speed operation.

The PRN components are restricted to 8 chip module assemblies only and are only approved for use on standard UDIMM module assemblies.

### ABSOLUTE MAXIMUM RATINGS:

Voltage on Vdd Supply relative to Vss .....-0.4V to 1.975V  
 Voltage on Vdd Supply relative to VssQ.....-0.4V to1.975V  
 Voltage on any pin relative to Vss.....-0.4V to1.975V  
 Operating Temperature T<sub>A</sub> (Ambient) ..... 0 ° to 95 °C  
 Storage Temperature ..... -55 to +150 °C

Stresses beyond the above listed parameters may cause permanent damage to the device. This is a stress only and functional operation of the device at or beyond these conditions is not implied. Exposure to these conditions for extended periods may affect device reliability.

## Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	32K (A[14:0])	32K (A[14:0])	16K (A[13:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

## Spectek Part Number Matrix

PRN256M8V79BG8GQF-15E

PRN: Spectek Branded Approved for 8 chip assemblies only

Component Depth: 256Mb

Component Width: x8

Design ID: V79B

Operating Voltage: G: 1.5V

Refresh rate: 8: 8K

Component package: GQ: 78/117B 8X10.5MM

Material type: F: Lead-free

Speed grade: -15E: PC3-10600 DDR3-1333

## FBGA Part Marking

PE 903 -15E

## Functional Description

DDR3 SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an  $8n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access consists of a single  $8n$ -bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding  $n$ -bit-wide, one-half-clock-cycle data transfers at the I/O pins.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITES. The read data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

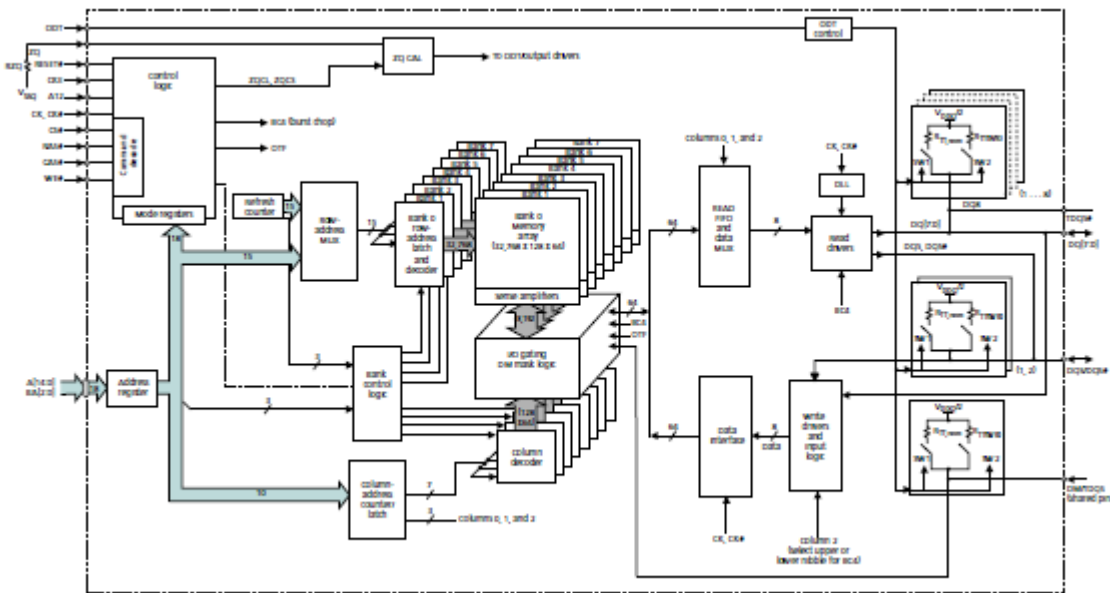
Read and write accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE commands are used to select the bank and the starting column location for the burst access.

The device uses a READ and WRITE BL8 and BC4. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard DDR SDRAM, the pipelined, multibank architecture of DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding row precharge and activation time.

A self refresh mode is provided, along with a power-saving, power-down mode.

Functional Block Diagram



### Ball Assignments and Descriptions 78 Ball FBGA X8 (Top view)

	1	2	3	4	5	6	7	8	9
A	○ V <sub>SS</sub>	○ V <sub>DD</sub>	○ NC				○ NF, NF/TDQ6#	○ V <sub>SS</sub>	○ V <sub>DD</sub>
B	○ V <sub>SS</sub>	○ V <sub>SSQ</sub>	● DQ0				○ DM, DM/TDQ5	○ V <sub>SSQ</sub>	○ V <sub>DDQ</sub>
C	○ V <sub>DDQ</sub>	● DQ2	○ DQ5				● DQ1	● DQ3	○ V <sub>SSQ</sub>
D	○ V <sub>SSQ</sub>	● NF, DQ6	○ DQ5#				○ V <sub>DD</sub>	○ V <sub>SS</sub>	○ V <sub>SSQ</sub>
E	○ V <sub>REFDQ</sub>	○ V <sub>DDQ</sub>	● NF, DQ4				● NF, DQ7	● NF, DQ5	○ V <sub>DDQ</sub>
F	○ NC	○ V <sub>SS</sub>	○ RAS#				○ CK	○ V <sub>SS</sub>	○ NC
G	○ ODT	○ V <sub>DD</sub>	○ CAS#				○ CK#	○ V <sub>DD</sub>	○ CKE
H	○ NC	○ CS#	○ WE#				● A10/AP	○ ZQ	○ NC
J	○ V <sub>SS</sub>	○ BA0	○ BA2				○ NC	○ V <sub>REFCA</sub>	○ V <sub>SS</sub>
K	○ V <sub>DD</sub>	● A3	● A0				● A12/BC#	○ BA1	○ V <sub>DD</sub>
L	○ V <sub>SS</sub>	● A5	● A2				● A1	● A4	○ V <sub>SS</sub>
M	○ V <sub>DD</sub>	● A7	● A9				● A11	● A6	○ V <sub>DD</sub>
N	○ V <sub>SS</sub>	○ RESET#	● A13				● A14	● A8	○ V <sub>SS</sub>

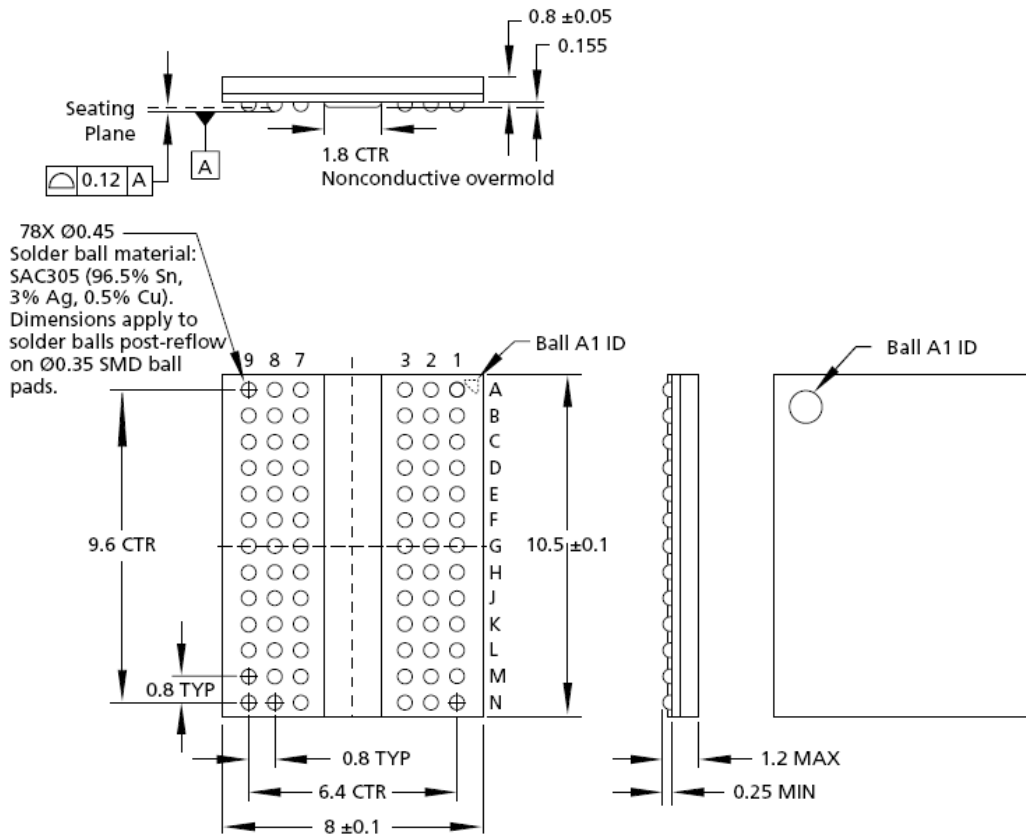
**Ball Descriptions**

Symbol	Type	Description
A[14:3], A12/BC#, A11, A10/AP, A[9:0]	Input	<b>Address inputs:</b> Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0] or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V <sub>ref-ca</sub> . A12/BC#: When enabled in the mode register (MR). A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop. LOW = BC4).
BA [2:0]	Input	<b>Bank address inputs:</b> BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2 or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V <sub>REFCA</sub> .
CK, CK#	Input	<b>Clock:</b> CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossing of CK and CK#.
CKE	Input	<b>CLOCK enable:</b> CKE ENABLES (registered HIGH) and disables (register LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET# and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. Cke is referenced to V <sub>REFCA</sub> .
CS#	Input	<b>Chip select:</b> CS# enables (register LOW) and disables (register HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V <sub>REFCA</sub> .
DM	Input	<b>Input data mask:</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with the input-only, the DM loading is designed to match that of the DQ and DQS balls. DM is referenced to V <sub>REFDQ</sub> . DM has an optional use as TDQS on the X8.
ODT	Input	<b>On-die termination:</b> ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls. DQ[7:0], DQS, DQS#, and DM for the X8; DQ[3:0], DQS, DQS# and DM for the X4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V <sub>REFCA</sub> .
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CS#, and WE# (along with CS#) define the command being entered and are referenced to V <sub>REFCA</sub> .
RESET#	Input	<b>Reset:</b> RESET# is an active LOW CMOS input referenced to VSS. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥0.8 X VDD and DC LOW ≤0.2 X VDDQ. RESET# assertin and de-assertin are asynchronous.

## Ball Descriptions Continued

Symbol	Type	Description
DQ[3:0]	I/O	<b>Data input/output:</b> Bidirectional data bus for the x4 configuration. DQ[3:0] are referenced to $V_{REFDQ}$ .
DQ[7:0]	I/O	<b>Data input/output:</b> Bidirectional data bus for the x8 configuration. DQ[7:0] are referenced to $V_{REFDQ}$ .
DQS, DQS#	I/O	<b>Data strobe:</b> Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
TDQS, TDQS#	Output	<b>Termination data strobe:</b> Applies to the x8 configuration only. When TDQS is enabled, DM is disabled, and the TDQS and TDQS# balls provide termination resistance.
$V_{DD}$	Supply	<b>Power supply:</b> 1.5V $\pm$ 0.075V.
$V_{DDQ}$	Supply	<b>DQ power supply:</b> 1.5V $\pm$ 0.075V. Isolated on the device for improved noise immunity.
$V_{REFCA}$	Supply	<b>Reference voltage for control, command, and address:</b> $V_{REFCA}$ must be maintained at all times (including self refresh) for proper device operation.
$V_{REFDQ}$	Supply	<b>Reference voltage for data:</b> $V_{REFDQ}$ must be maintained at all times (excluding self refresh) for proper device operation.
$V_{SS}$	Supply	Ground.
$V_{SSQ}$	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
ZQ	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to external 240 $\Omega$ resistor RZQ, which is tied to $V_{SSQ}$ .
NC	–	<b>No connect:</b> These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).
NF	–	<b>No function:</b> When configured as a x4 device, these balls are NF. When configured as a x8 device, these balls are defined as TDQS#, DQ[7:4].

**PRN256M8V79BG8GQF-15E**  
**V79B GQ: Package Dimensions : 78/117B 8X10.5MM**



Notes: 1. All dimensions are in millimeters.