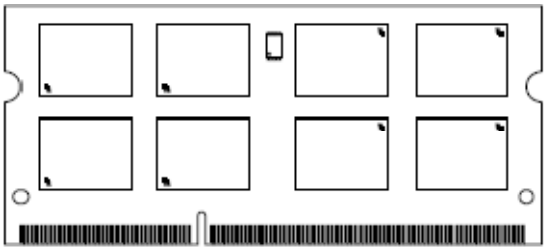
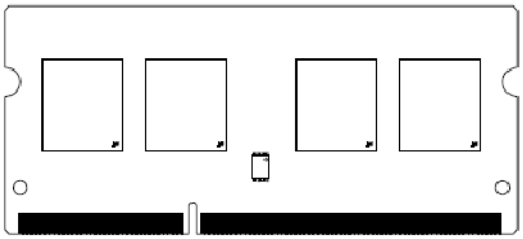
SDRAM DDR3 256M, 512M X 64 SODIMM

204-Pin 4GB SODIMM Assembly



204-Pin 2GB SODIMM Assembly



Features:

- DDR3 functionality and operations supported as defined in the component data sheet
- ROHS Complaint
- 204 pin small outline dual in-line memory module (SODIMM)
- Fast data transfer rates PC3-10600,
- Utilizes DDR3-1333 SDRAM FBGA components
- 2GB and 4GB (256MX64)
- Vdd = VddQ 1.5V ±0.75V,
- Nominal and Dynamic on-die termination (ODT) for data strobe and mask signals
- 8 internal device banks
- Adjustable data-output drive strength
- 64ms, 8,182 cycle refresh
- 7.8125us maximum average periodic refresh interval
- Gold edge connector contacts
- SERIAL Presence Detect (SPD)
- Terminated control, command and address bus

Options:

8 -256MX8 DDR3 SDRAM FBGA CHIPS
RN256M6408V69AS2J-XX DIE version D
RN256M6408V79DS2J-XX DIE version M

16 - 128MX8 DDR3 SDRAM FBGA CHIPS
RN512M6416V69AS2J-XX DIE version D
RN512M6416V79DS2J-XX DIE version M

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	Latencies CL-trcd-trp
-15E	-15E	667MHz	9-9-9

GENERAL DESCRIPTION

The RN256M6408V69AS2J, RN256M6408V79DS2J and RN512M64V69AS2J, RN512M6416V79DS2J are high performance dynamic random-access 2GB and 4GB modules respectively. These modules are organized in a x64 configuration, and utilize 8 bank architecture with a synchronous DDR interface. These DDR3 SDRAM modules use double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM DC RATINGS:

Voltage on Vdd Supply relative to Vss -1 to +2.3V
Voltage on VddQ Supply relative to Vss…..-0.5V to+2.3V
Voltage on VddL Supply relative to Vss…..-0.5V to+2.3V
Voltage on Vref and Inputs relative to Vss…..-1V to +3.6V
Voltage on I/O pins relative to Vss… -0.5V to VddQ +0.5V
Storage Temperature..... -55 to +150 °C

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Spectek Module Part Options and Designations

Options	Designation
Spectek Module	RN: Manufactured in USA
Module Depth & Width	
1GB	256M64
2GB	512M64
2 Digit chip count	
8 Chips	08
16 chips	16
Design ID	
Design revision	V69A (DIE VERSION D) V79D (DIE VERSION M)
Module type	
SODIMM	S
Component type	
X8	2
Package Type	
Lead Free FBGA	J
Leaded FBGA	B
Module Speed Grade	
DDR3 1333 PC3-10600	15E

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204 pin SODIMM Pin Assignments

204-Pin DDR3 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REFDQ}	53	DQ19	105	V_{DD}	157	DQ42
3	V_{SS}	55	V_{SS}	107	A10	159	DQ43
5	DQ0	57	DQ24	109	BA0	161	V_{SS}
7	DQ1	59	DQ25	111	V_{DD}	163	DQ48
9	V_{SS}	61	V_{SS}	113	WE#	165	DQ49
11	DM0	63	DM3	115	CAS#	167	V_{SS}
13	V_{SS}	65	V_{SS}	117	V_{DD}	169	DQS6#
15	DQ2	67	DQ26	119	A13	171	DQS6
17	DQ3	69	DQ27	121	S1#	173	V_{SS}
19	V_{SS}	71	V_{SS}	123	V_{DD}	175	DQ50
21	DQ8	73	CKE0	125	NC	177	DQ51
23	DQ9	75	V_{DD}	127	V_{SS}	179	V_{SS}
25	V_{SS}	77	NC	129	DQ32	181	DQ56
27	DQS1#	79	BA2	131	DQ33	183	DQ57
29	DQS1	81	V_{DD}	133	V_{SS}	185	V_{SS}
31	V_{SS}	83	A12	135	DQS4#	187	DM7
33	DQ10	85	A9	137	DQS4	189	V_{SS}
35	DQ11	87	V_{DD}	139	V_{SS}	191	DQ58
37	V_{SS}	89	A8	141	DQ34	193	DQ59
39	DQ16	91	A5	143	DQ35	195	V_{SS}
41	DQ17	93	V_{DD}	145	V_{SS}	197	SA0
43	V_{SS}	95	A3	147	DQ40	199	V_{DDSPD}
45	DQS2#	97	A1	149	DQ41	201	SA1
47	DQS2	99	V_{DD}	151	V_{SS}	203	V_{TT}
49	V_{SS}	101	CK0	153	DM5	–	–
51	DQ18	103	CK0#	155	V_{SS}	–	–

204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	V_{SS}	54	V_{SS}	106	V_{DD}	158	DQ46
4	DQ4	56	DQ28	108	BA1	160	DQ47
6	DQ5	58	DQ29	110	RAS#	162	V_{SS}
8	V_{SS}	60	V_{SS}	112	V_{DD}	164	DQ52
10	DQS0#	62	DQS3#	114	S0#	166	DQ53
12	DQS0	64	DQS3	116	ODT0	168	V_{SS}
14	V_{SS}	66	V_{SS}	118	V_{DD}	170	DM6
16	DQ6	68	DQ30	120	ODT1	172	V_{SS}
18	DQ7	70	DQ31	122	NC	174	DQ54
20	V_{SS}	72	V_{SS}	124	V_{DD}	176	DQ55
22	DQ12	74	CKE1	126	V_{REFCA}	178	V_{SS}
24	DQ13	76	V_{DD}	128	V_{SS}	180	DQ60
26	V_{SS}	78	NC	130	DQ36	182	DQ61
28	DM1	80	NC/A14	132	DQ37	184	V_{SS}
30	RESET#	82	V_{DD}	134	V_{SS}	186	DQS7#
32	V_{SS}	84	A11	136	DM4	188	DQS7
34	DQ14	86	A7	138	V_{SS}	190	V_{SS}
36	DQ15	88	V_{DD}	140	DQ38	192	DQ62
38	V_{SS}	90	A6	142	DQ39	194	DQ63
40	DQ20	92	A4	144	V_{SS}	196	V_{SS}
42	DQ21	94	V_{DD}	146	DQ44	198	EVENT#
44	V_{SS}	96	A2	148	DQ45	200	SDA
46	DM2	98	A0	150	V_{SS}	202	SCL
48	V_{SS}	100	V_{DD}	152	DQS5#	204	V_{TT}
50	DQ22	102	CK1	154	DQS5	–	–
52	DQ23	104	CK1#	156	V_{SS}	–	–

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PIN DESCRIPTIONS

The pin descriptions table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin assignments for information specific to this module.

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by Bax) or all banks (A10 HIGH). The address inputs also provide the op-code during a LEAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MRO, MR1, MR2 or MR3) is loaded during the LOAD MODE command.
CKx CKx#	Input	**Clock:** Differential clock inputs. All control command and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (register LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS. DQS#, DM and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS# and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS# and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) amd disables (registered HIGH) the command decoder.
SA#	Input	**Serial address inputs:** Used to configure the temperature senser/SPD EEPROM address range on the I2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data: edge-aligned with read data: input with read data: input with write data: center-aligned with write data

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Pin Descriptions (Continued)

The pin descriptions table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin assignments for information specific to this module.

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I2C bus.
TDQSx TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance: otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
Vdd	Supply	**Power supply:** 1.5V ±.075V. The component Vdd and Vddq are connected to the module Vdd.
VddSPD	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0V-3.6V.
Vrefca	Supply	**Reference voltage:** Control, commend and address Vdd/2.
Vrefdq	Supply	**Reference voltage:** DQ, DM, Vdd/2
Vss	Supply	Ground
Vtt	Supply	**Termination voltage:** Used for control, command and address Vd/2
NC	-	**No connect:** These pins are not connected on the module
NF	-	**No function:** These pins are connected within the module, but provide no functionality.

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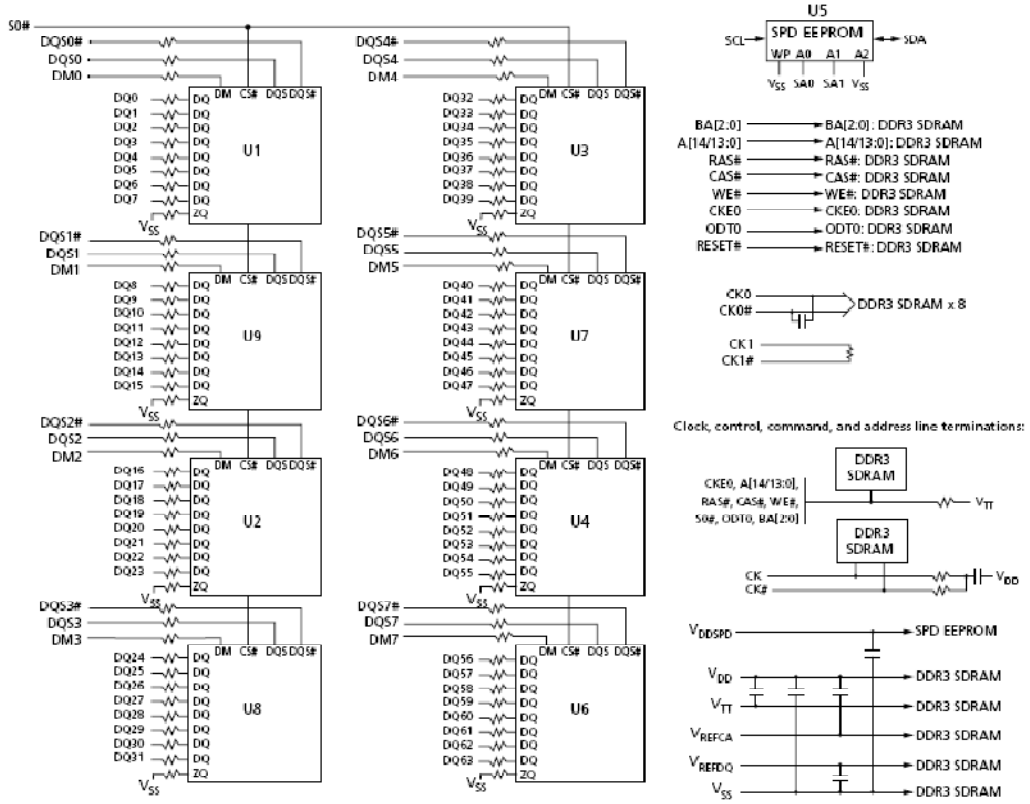
2GB functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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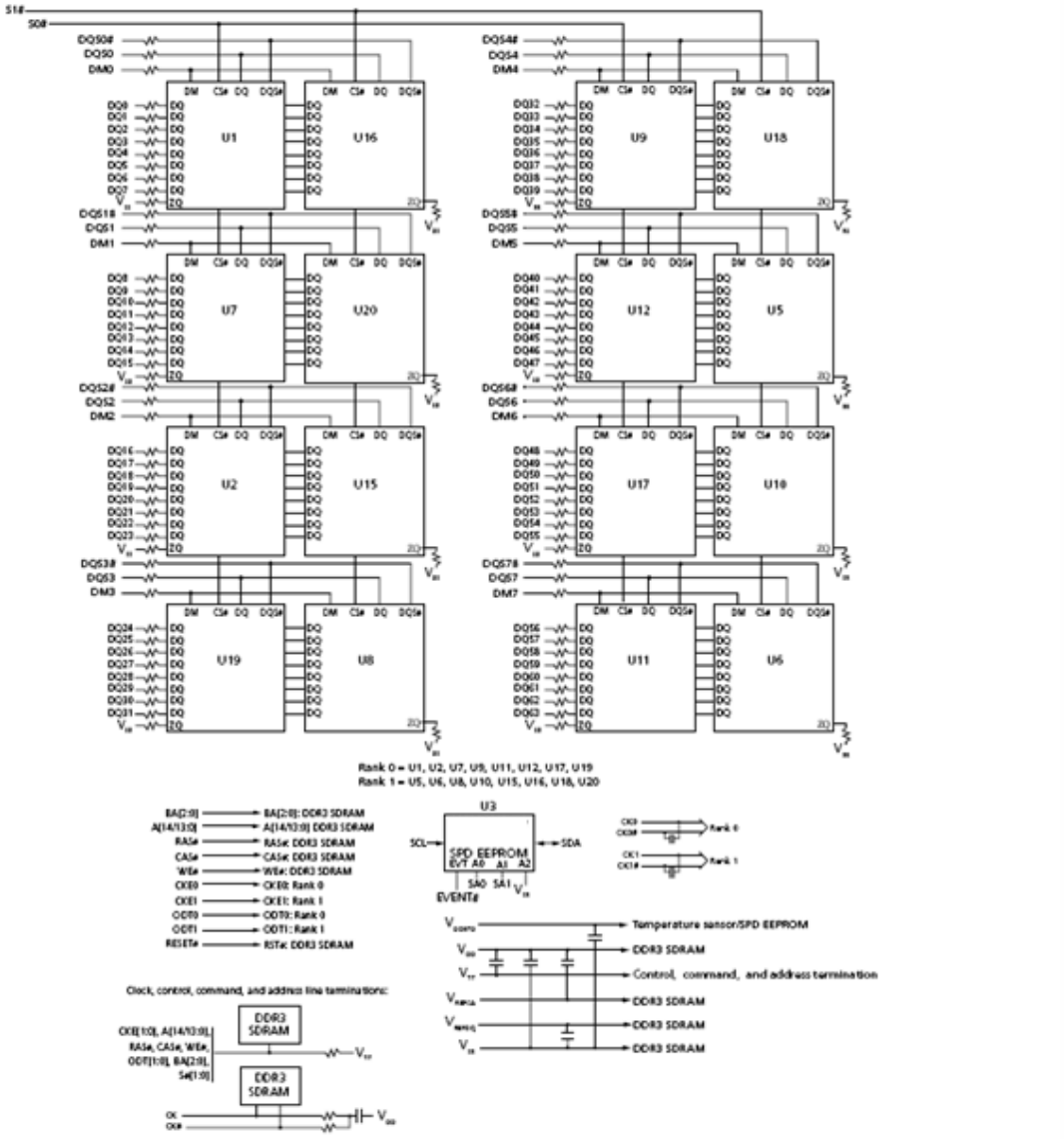
4GB functional Block Diagram



Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

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Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	600	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus		0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	1
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs, RAS#, CAS#, WE#, S#, CKE, ODT, BA, CK, CK#	–16	0	16	µA	
		DM	–2	0	2		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DD}; DQ and ODT are disabled; ODT is HIGH	DQ, DQS, DQS#	–5	0	5	µA	
I_{VREF}	V_{REF} supply leakage current; $V_{REF}DQ = V_{DD}/2$ or $V_{REFCA} = V_{DD}/2$ (All other pins not under test = 0V)		–8	0	8	µA	
T_A	Module ambient operating temperature	Commercial	0	–	70	°C	2, 3
		Industrial	–40	–	85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	95	°C	2, 3, 4
		Industrial	–40	–	95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

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IDD Specifications and Conditions 2GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev D.

Parameter	Symbol	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	680	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	800	mA
Precharge power down current: Slow exit	Idd2p0	96	mA
Precharge power down current: Fast exit	Idd2p1	240	mA
Precharge quiet standby current	Idd2Q	280	mA
Precharge standby current	Idd2N	296	mA
Precharge standby ODT current	Idd2NT	360	mA
Active power down standby current	Idd3P	280	mA
Active standby current	Idd3N	320	mA
Burst read operating current	Idd4R	1280	mA
Burst write operating current	Idd4w	1320	mA
Refresh current	Idd5B	1600	mA
Self refresh temperature current: MAX Tc=85C	Idd6	96	mA
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	120	mA
All banks interleaved read current	Idd7	3080	mA
Reset current	Idd8	112	mA

IDD Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev D.

Parameter	Symbol	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	776	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	896	mA
Precharge power down current: Slow exit	Idd2p0	192	mA
Precharge power down current: Fast exit	Idd2p1	480	mA
Precharge quiet standby current	Idd2Q	560	mA
Precharge standby current	Idd2N	592	mA
Precharge standby ODT current	Idd2NT	456	mA
Active power down standby current	Idd3P	560	mA
Active standby current	Idd3N	640	mA
Burst read operating current	Idd4R	1376	mA
Burst write operating current	Idd4w	1416	mA
Refresh current	Idd5B	1696	mA
Self refresh temperature current: MAX Tc=85C	Idd6	192	mA
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	240	mA
All banks interleaved read current	Idd7	3176	mA
Reset current	Idd8	224	mA

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IDD Specifications and Conditions 2GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev M.

Parameter	Symbol	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	520	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	600	mA
Precharge power down current: Slow exit	Idd2p0	96	mA
Precharge power down current: Fast exit	Idd2p1	256	mA
Precharge quiet standby current	Idd2Q	280	mA
Precharge standby current	Idd2N	304	mA
Precharge standby ODT current	Idd2NT	320	mA
Active power down standby current	Idd3P	360	mA
Active standby current	Idd3N	400	mA
Burst read operating current	Idd4R	1128	mA
Burst write operating current	Idd4w	1040	mA
Refresh current	Idd5B	1520	mA
Self refresh temperature current: MAX Tc=85C	Idd6	96	mA
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	120	mA
All banks interleaved read current	Idd7	1800	mA
Reset current	Idd8	112	mA

IDD Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev M.

Parameter	Symbol	1333	Units
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	616	mA
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	696	mA
Precharge power down current: Slow exit	Idd2p0	192	mA
Precharge power down current: Fast exit	Idd2p1	512	mA
Precharge quiet standby current	Idd2Q	560	mA
Precharge standby current	Idd2N	608	mA
Precharge standby ODT current	Idd2NT	416	mA
Active power down standby current	Idd3P	720	mA
Active standby current	Idd3N	800	mA
Burst read operating current	Idd4R	1224	mA
Burst write operating current	Idd4w	1136	mA
Refresh current	Idd5B	1616	mA
Self refresh temperature current: MAX Tc=85C	Idd6	192	mA
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	216	mA
All banks interleaved read current	Idd7	1896	mA
Reset current	Idd8	208	mA

Addressing

Parameter	2GB	4GB
Refresh count	8k	8K
Row address	16K A(14:0)	16K A(14:0)
Device bank address	8 BA [2:0]	8 BA [2:0]
Device page size per bank	1KB	1KB
Device configuration	2Gb (256M X8)	2Gb (256M X8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	2 S# [1:0]	2 S# [1:0]

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SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

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Serial Presence- Detect EEPROM

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} + 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} + 0.7	V_{DDSPD} + 1.0	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	2.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	2.0	µA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	^{t}SCL	10	400	kHz	
Clock pulse width high time	^{t}HIGH	0.6	–	µs	
Clock pulse width low time	^{t}LOW	1.3	–	µs	
SDA rise time	^{t}R	–	300	µs	1
SDA fall time	^{t}F	20	300	ns	1
Data-in setup time	^{t}SU:DAT	100	–	ns	
Data-in hold time	^{t}HD:DI	0	–	µs	
Data-out hold time	^{t}HD:DAT	200	900	ns	
Data out access time from SCL low	^{t}AA:DAT	0.2	0.9	µs	2
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
WRITE time	^{t}W	–	10	ms	

Notes:
1. Guaranteed by design and characterization, not necessarily tested.
2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
3. For a restart condition, or following a WRITE cycle.

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