SDRAM DDR3 256M, 512M X 64 UDIMM

Features:

- DDR3 functionality and operations supported as per component data sheet
- ROHS Complaint
- 240 pin unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rates PC3-10600,
- Utilizes DDR3-1333 SDRAM FBGA components
- 2GB (256MX64), 4GB (512MX64)
- Vdd = VddQ 1.5V ±0.75V,
- Adjustable data-output drive strength
- Addresses are mirrored for second rank
- 64ms, 8,182 cycle refresh
- 7.8125us maximum average periodic refresh interval
- Gold edge connector contacts
- SERIAL Presence Detect (SPD)
- Terminated control, command and address bus

Options:

8 -256Mx8 DDR3 SDRAM FBGA CHIPS
RN256M6408V69AD2J-XX DIE version D
RN256M6408V79DD2J-XX DIE version M

16 - 256MX8 DDR3 SDRAM FBGA CHIPS
RN512M6416V69AD2J-XX DIE version D
RN512M6416V79DD2J-XX DIE version M

KEY DIMM MODULE TIMING PARAMETERS

Module Marking	Component Marking	Clock Frequency	Latencies
-15E	-15E	667MHz	9-9-9

GENERAL DESCRIPTION

The RN256M6408V69AD2J, RN256M6408V79DD2J and RN512M6416V69AD2J, RN512M6416V79DD2J are high performance dynamic random-access 2GB and 4GB modules respectively. These modules are organized in a x64 configuration, and utilize 8 bank architecture with a synchronous DDR interface. These DDR3 SDRAM modules use double data rate architecture to achieve high speed operation.

ABSOLUTE MAXIMUM DC RATINGS:

Voltage on Vdd Supply relative to Vss.....-1 to +2.3V
Voltage on VddQ Supply relative to Vss.....-0.5V to+2.3V
Voltage on VddL Supply relative to Vss.....-0.5V to+2.3V
Voltage on Vref and Inputs relative to Vss.....-1V to +3.6V
Voltage on I/O pins relative to Vss… -0.5V to VddQ +0.5V
Storage Temperature.....-55 to +150 °C

PIN ASSIGNMENT
240-Pin UDIMM

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	Vrefdq	61	A2	121	Vss	181	A1
2	Vss	62	Vdd	122	DQ4	182	Vdd
3	DQ0	63	CK1	123	DQ5	183	Vdd
4	DQ1	64	CK1#	124	Vss	184	CK0
5	Vss	65	Vdd	125	DM0	185	CK0#
6	DQSO#	66	Vdd	126	NC	186	Vdd
7	DQS0	67	Vrefca	127	Vss	187	NC
8	Vss	68	NC	128	DQ6	188	A0
9	DQ2	69	Vdd	129	DQ7	189	Vdd
10	DQ3	70	A10	130	Vss	190	BA1
11	Vss	71	BA0	131	DQ12	191	Vdd
12	DQ8	72	Vdd	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	Vss	193	S0#
14	Vss	74	CAS#	134	DM1	194	Vdd
15	DQS1#	75	Vdd	135	NC	195	ODT0
16	DQS1	76	S1#	136	Vss	196	A13
17	Vss	77	ODT1	137	DQ14	197	Vdd
18	DQ10	78	Vdd	138	DQ15	198	NC
19	DQ11	79	NC	139	Vss	199	Vss
20	Vss	80	Vss	140	DQ20	200	DQ36
21	DQ16	81	DQ32	141	DQ21	201	DQ37
22	DQ17	82	DQ33	142	Vss	202	Vss
23	Vss	83	Vss	143	DM2	203	DM4
24	DQS2#	84	DQS4#	144	NC	204	NC
25	DQS2	85	DQS4	145	Vss	205	Vss
26	Vss	86	Vss	146	DQ22	206	DQ38
27	DQ18	87	DQ34	147	DQ23	207	DQ39
28	DQ19	88	DQ35	148	Vss	208	Vss
29	Vss	89	Vss	149	DQ28	209	DQ44
30	DQ24	90	DQ40	150	DQ29	210	DQ45
31	DQ25	91	DQ41	151	Vss	211	Vss
32	Vss	92	Vss	152	DM3	212	DM5
33	DQS3#	93	DQS5#	153	NC	213	NC
34	DQS3	94	DQS5	154	Vss	214	Vss
35	Vss	95	Vss	155	DQ30	215	DQ46
36	DQ26	96	DQ42	156	DQ31	216	DQ47
37	DQ27	97	DQ43	157	Vss	217	Vss
38	Vss	98	Vss	158	NC	218	DQ52
39	NC	99	DQ48	159	NC	219	DQ53
40	NC	100	DQ49	160	Vss	220	Vss
41	Vss	101	Vss	161	NC	221	DM6
42	NC	102	DQS6#	162	NC	222	NC
43	NC	103	DQS6	163	Vss	223	Vss
44	Vss	104	Vss	164	NC	224	DQ54
45	NC	105	DQ50	165	NC	225	DQ55
46	NC	106	DQ51	166	Vss	226	Vss
47	Vss	107	Vss	167	NC	227	DQ60
48	NC	108	DQ56	168	RESET#	228	DQ61
49	NC	109	DQ57	169	CKE1	229	Vss
50	CKE0	110	Vss	170	Vdd	230	DM7
51	VDD	111	DQS7#	171	NC	231	NC
52	BA2	112	DQS7	172	NC	232	Vss
53	NC	113	Vss	173	Vdd	233	DQ62
54	Vdd	114	DQ58	174	A12	234	DQ63
55	A11	115	DQ59	175	A9	235	Vss
56	A7	116	Vss	176	Vdd	236	Vddpd
57	Vdd	117	SA0	177	A8	237	SA1
58	A5	118	SCL	178	A6	238	SDA
59	A4	119	SA2	179	Vdd	239	Vss
60	Vdd	120	Vtt	180	A3	240	Vtt

Spectek Module Part Options and Designations

Options	Designation
Spectek Module	RN: Manufactured in USA
Module Depth & Width	
2GB	256M64
4GB	512M64
2 Digit chip count	
8 Chips	08
16 chips	16
Design ID	
Design revision	V69A (DIE version D) V79D (DIE version M)
Module type	
UDIMM	D
Component type	
X8	2
Package Type	
Lead Free FBGA	J
Module Speed Grade	
DDR3 1333 PC3-10600	15E

Pin Descriptions

The pin descriptions table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin assignments for information specific to this module.

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by Bax) or all banks (A10 HIGH). The address inputs also provide the op-code during a LEAD MODE command. See the Pin Assignments Table for density-specific addressing information.
BAx	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MRO, MR1, MR2 or MR3) is loaded during the LOAD MODE command.
CKx CKx#	Input	**Clock:** Differential clock inputs. All control command and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
DMx	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODTx	Input	**On-die termination:** Enables (registered HIGH) and disables (register LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS. DQS#, DM and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
Par_In	Input	**Parity input:** Parity bit for Ax, RAS#, CAS# and WE#.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS# and WE# (along with S#) define the command being entered.
RESET#	Input (LVCMOS)	**Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed.
Sx#	Input	**Chip select:** Enables (registered LOW) amd disables (registered HIGH) the command decoder.
SA#	Input	**Serial address inputs:** Used to configure the temperature senser/SPD EEPROM address range on the I2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus.
CBx	I/O	**Check bits:** Used for system error detection and correction.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQSx DQSx#	I/O	**Data strobe:** Differential data strobes. Output with read data: edge-aligned with read data: input with read data: input with write data: center-aligned with write data

Pin Descriptions - Continued)

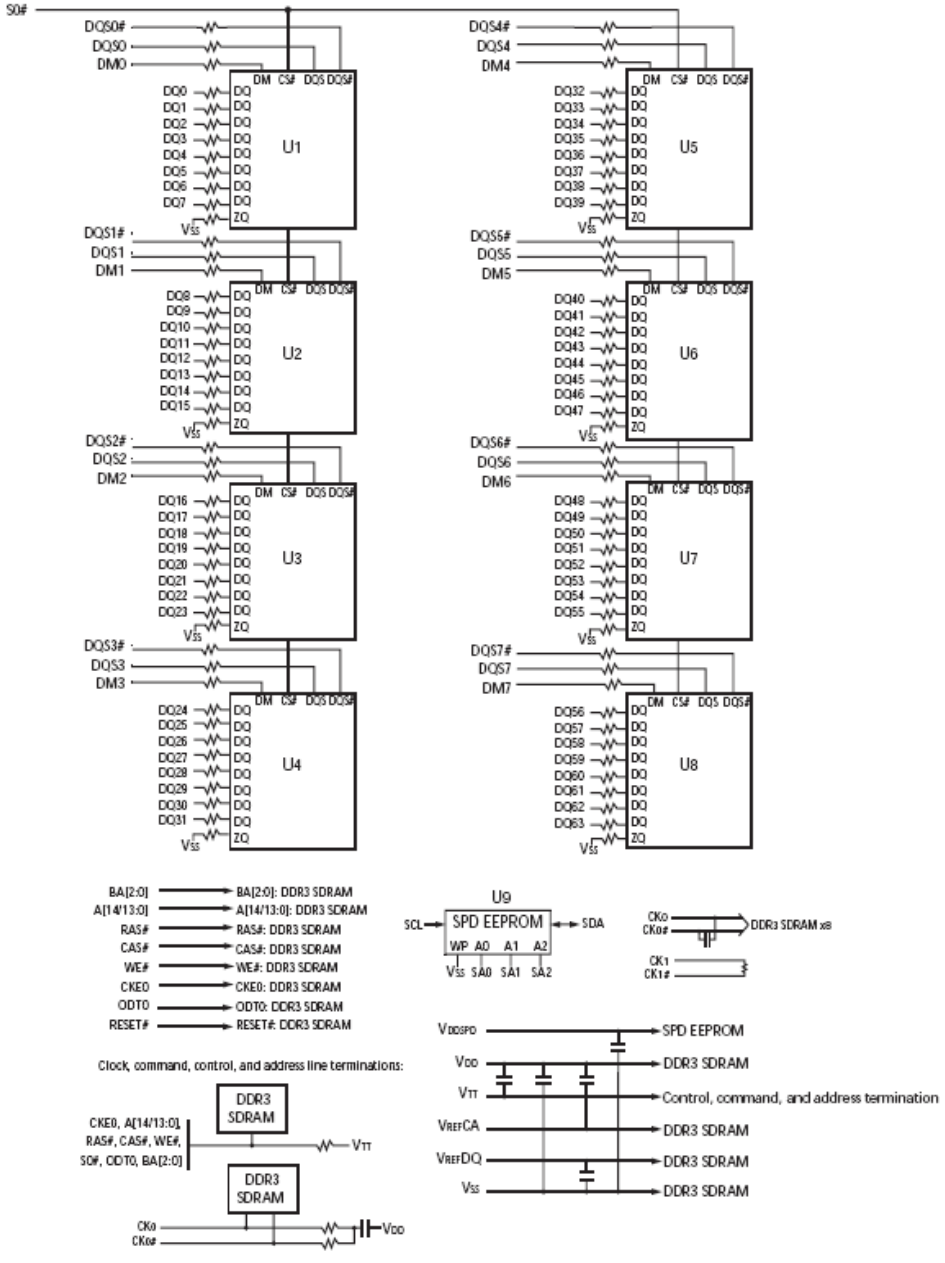
The pin descriptions table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin assignments for information specific to this module.

Symbol	Type	Description
SDA	I/O	**Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the I2C bus.
TDQSx TDQSx#	Output	**Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance: otherwise, TDQS# are no function.
Err_Out#	Output (open drain)	**Parity error output:** Parity error found on the command and address bus.
EVENT#	Output (open drain)	**Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded.
Vdd	Supply	**Power supply:** 1.5V ±.075V. The component Vdd and Vddq are connected to the module Vdd.
VddSPD	Supply	**Temperature sensor/SPD EEPROM power supply:** 3.0V-3.6V.
Vrefca	Supply	**Reference voltage:** Control, commend and address Vdd/2.
Vrefdq	Supply	**Reference voltage:** DQ, DM, Vdd/2
Vss	Supply	Ground
Vtt	Supply	**Termination voltage:** Used for control, command and address Vd/2
NC	-	**No connect:** These pins are not connected on the module
NF	-	**No function:** These pins are connected within the module, but provide no functionality.

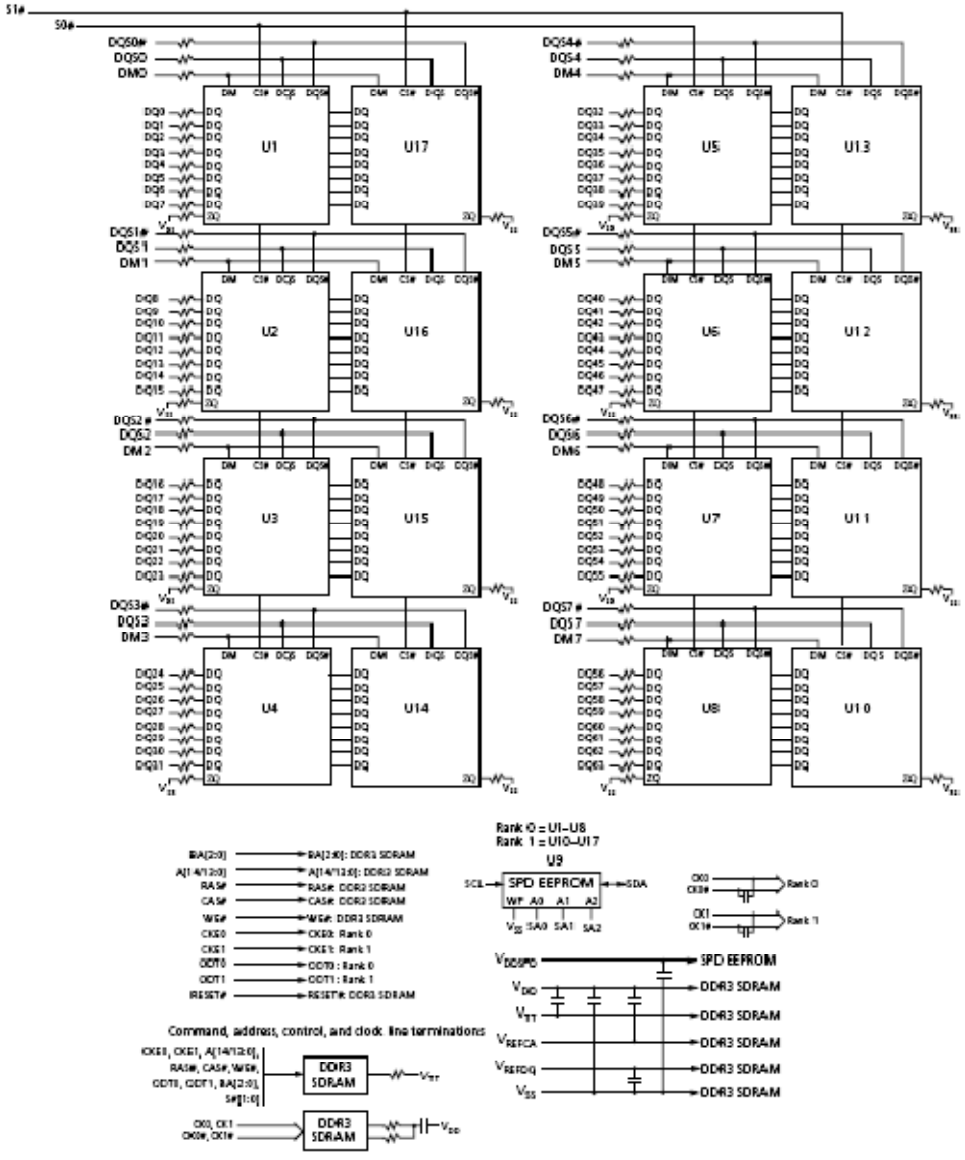
Addressing

Parameter	2GB	4GB
Refresh count	8k	8K
Row address	16K A(14:0)	16K A(14:0)
Device bank address	8 BA [2:0]	8 BA [2:0]
Device page size per bank	1KB	1KB
Device configuration	2Gb (256M X8)	2Gb (256M X8)
Column address	1K A[9:0]	1K A[9:0]
Module rank address	2 S# [1:0]	2 S# [1:0]

2GB Functional Block Diagram



4GB Functional Block Diagram



General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially a 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to V_{SS}, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	+1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	+1.975	V

Table 9: Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage		1.425	1.5	1.575	V	
I_{VTT}	Termination reference current from V_{TT}		–600	–	+600	mA	
V_{TT}	Termination reference voltage – command address bus		0.483 x V_{DD}	0.5 x V_{DD}	0.517 x V_{DD}	V	1
I_I	Input leakage current; Any input 0V ≤ V_{IN} ≤ V_{DD}; V_{REF} input 0V ≤ V_{IN} ≤ 0.95V (All other pins not under test = 0V)	Address inputs RAS#, CAS#, WE#, BA	–32	0	+32	µA	
		S#, CKE, ODT, CK, CK#	–16	0	+16		
		DM	–4	0	+4		
I_{OZ}	Output leakage current; 0V ≤ V_{OUT} ≤ V_{DDQ}; DQs and ODT are disabled	DQ, DQS, DQS#	–10	0	+10	µA	
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level		–16	0	+16	µA	
T_A	Module ambient operating temperature	Commercial	0	–	+70	°C	2, 3
		Industrial	–40	–	+85	°C	
T_C	DDR3 SDRAM component case operating temperature	Commercial	0	–	+85	°C	2, 3, 4
		Industrial	–40	–	+95	°C	

Notes:
1. V_{TT} termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
2. T_A and T_C are simultaneous requirements.
3. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
4. The refresh rate is required to double when 85°C < T_C ≤ 95°C.

IDD Specifications and Conditions 2GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev D.

Parameter	Symbol	1333
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	680
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	800
Precharge power down current: Slow exit	Idd2p0	96
Precharge power down current: Fast exit	Idd2p1	240
Precharge quiet standby current	Idd2Q	280
Precharge standby current	Idd2N	296
Precharge standby ODT current	Idd2NT	360
Active power down standby current	Idd3P	280
Active standby current	Idd3N	320
Burst read operating current	Idd4R	1280
Burst write operating current	Idd4w	1320
Refresh current	Idd5B	1600
Self refresh temperature current: MAX Tc=85C	Idd6	96
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	120
All banks interleaved read current	Idd7	3080
Reset current	Idd8	112

IDD Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev D.

Parameter	Symbol	1333
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	776
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	896
Precharge power down current: Slow exit	Idd2p0	192
Precharge power down current: Fast exit	Idd2p1	480
Precharge quiet standby current	Idd2Q	560
Precharge standby current	Idd2N	592
Precharge standby ODT current	Idd2NT	456
Active power down standby current	Idd3P	560
Active standby current	Idd3N	640
Burst read operating current	Idd4R	1376
Burst write operating current	Idd4w	1416
Refresh current	Idd5B	1696
Self refresh temperature current: MAX Tc=85C	Idd6	192
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	240
All banks interleaved read current	Idd7	3176
Reset current	Idd8	224

IDD Specifications and Conditions 2GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev M.

Parameter	Symbol	1333
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	520
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	600
Precharge power down current: Slow exit	Idd2p0	96
Precharge power down current: Fast exit	Idd2p1	256
Precharge quiet standby current	Idd2Q	280
Precharge standby current	Idd2N	304
Precharge standby ODT current	Idd2NT	320
Active power down standby current	Idd3P	360
Active standby current	Idd3N	400
Burst read operating current	Idd4R	1128
Burst write operating current	Idd4w	1040
Refresh current	Idd5B	1520
Self refresh temperature current: MAX Tc=85C	Idd6	96
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	120
All banks interleaved read current	Idd7	1800
Reset current	Idd8	112

IDD Specifications and Conditions – 4GB

Values are for the MT41J256M8 DDR3 SDRAM only and are computed from values specified in the 2Gb 256mx8 component data sheet, Die Rev M.

Parameter	Symbol	1333
Operating current 0: One bank ACTIVATE-to-PRECHARGE	Idd0	616
Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE	Idd1	696
Precharge power down current: Slow exit	Idd2p0	192
Precharge power down current: Fast exit	Idd2p1	512
Precharge quiet standby current	Idd2Q	560
Precharge standby current	Idd2N	608
Precharge standby ODT current	Idd2NT	416
Active power down standby current	Idd3P	720
Active standby current	Idd3N	800
Burst read operating current	Idd4R	1224
Burst write operating current	Idd4w	1136
Refresh current	Idd5B	1616
Self refresh temperature current: MAX Tc=85C	Idd6	192
Self refresh temperature current (SRT enabled): MAXTc=95C	Idd6ET	216
All banks interleaved read current	Idd7	1896
Reset current	Idd8	208

SERIAL PRESENCE-DETECT OPERATION - This module incorporates Serial Presence-Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM, containing 256 bytes of nonvolatile storage. The first 128 bytes can be programmed by SpecTek to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide 8 unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS - Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION - All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The serial PD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION - All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition also places the serial PD device into standby power mode.

SPD ACKNOWLEDGE - Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits of data (Figure 3). The PD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the PD device will respond with an acknowledge after the receipt of each subsequent eight bit word. In the read mode the PD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Serial Presence – Detect EEPROM

All voltages referenced to V_{DDSPD}

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	V_{DDSPD}	3.0	3.6	V
Input low voltage: Logic 0; All inputs	V_{IL}	–0.6	V_{DDSPD} + 0.3	V
Input high voltage: Logic 1; All inputs	V_{IH}	V_{DDSPD} + 0.7	V_{DDSPD} + 1.0	V
Output low voltage: I_{OUT} = 3mA	V_{OL}	–	0.4	V
Input leakage current: V_{IN} = GND to V_{DD}	I_{LI}	0.1	2.0	µA
Output leakage current: V_{OUT} = GND to V_{DD}	I_{LO}	0.05	2.0	µA

Table 14: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock frequency	^{t}SCL	10	400	kHz	
Clock pulse width high time	^{t}HIGH	0.6	–	µs	
Clock pulse width low time	^{t}LOW	1.3	–	µs	
SDA rise time	^{t}R	–	300	µs	1
SDA fall time	^{t}F	20	300	ns	1
Data-in setup time	^{t}SU:DAT	100	–	ns	
Data-in hold time	^{t}HD:DI	0	–	µs	
Data-out hold time	^{t}HD:DAT	200	900	ns	
Data out access time from SCL low	^{t}AA:DAT	0.2	0.9	µs	2
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Start condition hold time	^{t}HD:STA	0.6	–	µs	
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
WRITE time	^{t}W	–	10	ms	

Notes:
1. Guaranteed by design and characterization, not necessarily tested.
2. To avoid spurious start and stop conditions, a minimum delay is placed between the falling edge of SCL and the falling or rising edge of SDA.
3. For a restart condition, or following a WRITE cycle.