SDRAM DDR2 128MX8 ½ Density Device Technical Note

Introduction

This technical note provides an overview of how the SGG64M8U68AOACCF-25L DDR3 SDRAM device is configured and tested as a half good 1Gb device.
This device is tested and configured as a 64MX8 512Mb device using BA2.
BA2 must be connected to ground in order to utilize this device to its intended density and configuration.
With BA2 connected to ground the device will function as a 64MX8 full good device.
Running this device without ground BA2 will result in unstable operation.

Addressing

Parameter	1Gb ½ Density Device Configuration 64M X8	1Gb Device Configuration for reference only 128M X 8
Configuration	16MEG X 8 X 4 Banks	16MEG X 8 X 8 banks
Refresh count	8K	8K
Row addressing	16K A0-A13	16K A0-A13
Bank addressing	4: BA0-BA1 4: BA2=GND	8: BAO-BA2
Column addressing	1K A0-A9	1K A0-A9

Refer to the 1Gb DDR2 SDRAM Datasheet for all other AC and DC timing parameters.

Spectek Component Part Options and Designations

Options	Designation
Spectek Memory	**SGG Spectek Component sales**
Component depth	**64MEG**
Component width	**x8**
Design ID	**U68A (1/2 density device)**
Operating voltage	**1.8V**
Refresh	**A: 8K**
Component package type:	**CC: 60/99B 8x10MM**
Material type	**F: LEAD-FREE**
Device speed	**-25L 800MHz 6-6-6-1.8v Lower good by BA2=0**

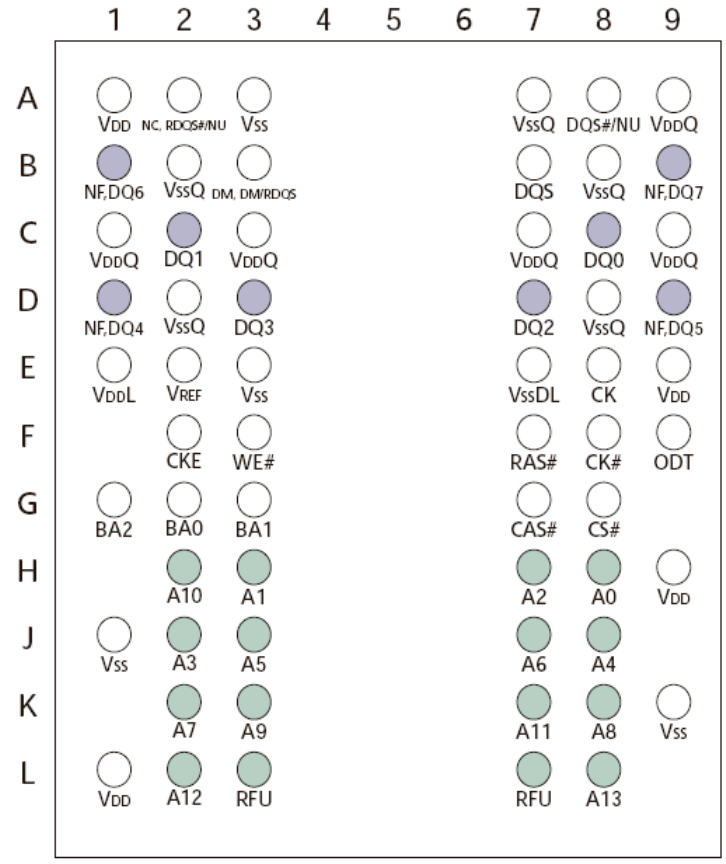
Pin Descriptions

Symbol	Type	Description
A0-A13	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by Bax) or all banks (A10 HIGH). The address inputs also provide the op-code during a LEAD MODE command.
BA0-BA1	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MRO, MR1, MR2 or MR3) is loaded during the LOAD MODE command.
BA2	Input	**Bank address BA2 input:** Must be connected to GND for ½ density operation. BA2 must also be connected to GND to insure stable operation.
CKx CKx#	Input	**Clock:** Differential clock inputs. All control command and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKEx	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with moltiple ranks. CS# is considered part of the command code.
DM	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODT	Input	**On-die termination:** Enables (registered HIGH) and disables (register LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS. DQS#, DM and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS# and WE# (along with CS#) define the command being entered.
DQx	I/O	**Data input/output:** Bidirectional data bus.
DQS DQS#	I/O	**Data strobe:** Differential data strobes. Output with read data: edge-aligned with read data: input with read data: input with write data: center-aligned with write data

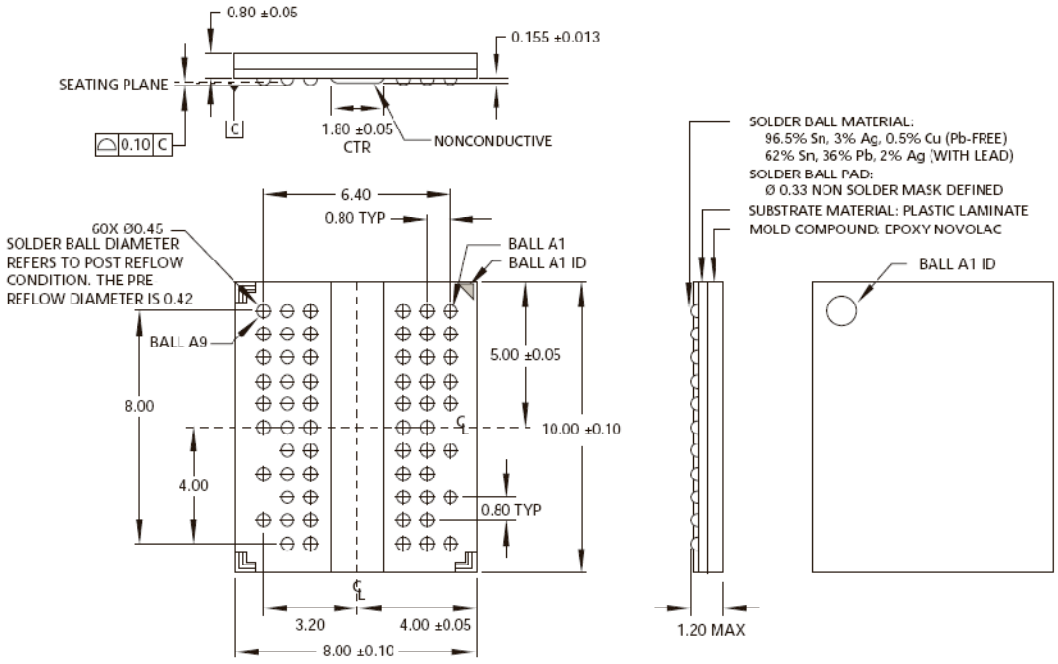
Pin Descriptions - Continued)

Symbol	Type	Description
RDQS RDQSx#	Output	**Redundant data strobe (x8 devices only):** RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance: otherwise, TDQS# are no function.
Vdd	Supply	**Power Supply:** 1.8V ±0.1V.
VddQ	Supply	**DQ Power Supply:** 1.8V ±0.1V Isolated on the device for improved noise immunity.
VddL	Supply	**DLL Power Supply:** 1.8V ±0.1V
Vref	Supply	**Reference voltage:** SSTL_18 reference voltage
Vss	Supply	Ground
VssDL	Supply	**DLL ground:** Isolated on the device from Vss and VssQ
VssQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NC	-	**No connect:** These pins are not connected on the module
NF	-	**No function:** These pins are connected within the module, but provide no functionality.
NU	-	**Not used: For x8 only**
RFU	-	**Reserved for future use**

Ball Assignments and Descriptions
60 – Ball FBGA X8 (Top View)



60 – Ball FBGA Package 8MM X 10MM x8



Notes: 1. All dimensions are in millimeters.