SDRAM DDR3 512MX8 ½ Density Device Technical Note

Introduction

This technical note provides an overview of how the XAA512M82C0CG8GRF-SSHO and SSH1 DDR3 SDRAM device is configured and tested as a 2Gb device.

Addressing

Parameter	4Gb ½ Density Device Configuration 2Gb 256M X8	4Gb Device Configuration for reference only 4Gb 512M X 8
Configuration	32MEG X 8 X 8 Banks	64MEG X 8 X 8 Banks
Refresh count	8K	8K
Row addressing	64K A0-A15	64K A0-A15
SSH0 ½ Density addressing	A15=0	N/A
SSH1 ½ Density addressing	A15=1	N/A
Bank addressing	8: BA0-BA2	8: BAO-BA2
Column addressing	2K A0-A9,11	1K A0-A9,11
Page Size	1KB	1KB

For ½ Density opperation address A15 must be configured as follows:
The SSH0 and SSH1 devices are fully tested as density full good as follows.
SSH0 address A15 must be tied to ground
SSH1 address A15 must be tied to Vdd.

Reference the 4Gb device datasheet for actual timing and IDD parameters

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Spectek Component Part Options and Designations

Options	**Designation**
Spectek Memory	**XAA Generic Component sales**
Address A15=0 or A15=1	
Component depth	**256MEG**
Component width	**x8**
Design ID	**2C0C (1/2 density device)**
Operating voltage	**1.5V**
Refresh	**8: 8K**
Component package type:	**GR: 78/117B 9X10.6MM**
Material type	**F: LEAD-FREE**
Device speed	**SSH0 A15=0** **SSH1 A15=1**

Pin Descriptions

Symbol	Type	Description
A0-A15	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to Vrefca. A12: When enable in the mode register (MR), A12 is sampled during READ adn WRTIE commands to determne whether burst chop (on-the-fly) will be perfrmed (HIGH = BL8 or no burst chop, LOW = BC4)
BA0-BA2	Input	**Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MRO, MR1, MR2 or MR3) is loaded during the LOAD MODE command.BA[2:0] are reference to Vrefca
CKx CKx#	Input	**Clock:** Differential clock inputs. All control command and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS,DSS#) is referenced to crossings of CK and CK#.
CKE	Input	**Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
DM	Input	**Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODT	Input	**On-die termination:** Enables (registered HIGH) and disables (register LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS. DQS#, DM and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS# and WE# (along with CS#) define the command being entered.
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to rail signal wiht DC HIGH $\geq$0.8 x Vdd and DC LOW $\leq$ 0.2X Vddq. RESET# asserion and deseerion are asynchronous.
DQ0- DQ7	I/O	**Data input/output:** Bidirectional data bus.
DQS DQS#	I/O	**Data strobe:** Differential data strobes. Output with read data: edge-aligned with read data: input with read data: input with write data: center-aligned with write data

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Pin Descriptions - Continued)

Symbol	Type	Description
TDQS TDQSx#	Output	**Termination data strobe (x8 devices only)** When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance:.
Vdd	Supply	**Power Supply:** 1.5V $\underline{+}$0.1V.
VddQ	Supply	**DQ Power Supply:** 1.5V $\underline{+}$0.1V Isolated on the device for improved noise immunity.
Vddrefca	Supply	**Reference voltage for control, command and address:** Vrefca must be maintained at all times (including self refresh) for proper device operation.
Vrefdq	Supply	**Reference voltage for data:** Vrefdq must be maintained at all times (excluding self refresh) for proper device operation.
Vss	Supply	Ground
VssQ	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240 ohm resistor (RZQ) which is tied to Vssq.
NC	-	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls)
NF	-	**No function:** When configured as X4 device, these balls are NF. When configured as X8 device, these balls are defined as TDQS#,DQ[7:4].

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Ball Assignments and Descriptions
78 – Ball FBGA X8 (Top View)

	1	2	3	4	5	6	7	8	9
A	VSS	VDD	NC				NF, NF/TDQS#	VSS	VDD
B	VSS	VSSQ	DQ0				DM, DM/TDQS	VSSQ	VDDQ
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ
D	VSSQ	NF, DQ6	DQS#				VDD	VSS	VSSQ
E	VREFDQ	VDDQ	NF, DQ4				NF, DQ7	NF, DQ5	VDDQ
F	NC	VSS	RAS#				CK	VSS	NC
G	ODT	VDD	CAS#				CK#	VDD	CKE
H	NC	CS#	WE#				A10/AP	ZQ	NC
J	VSS	BA0	BA2				NC	VREFCA	VSS
K	VDD	A3	A0				A12/BC#	BA1	VDD
L	VSS	A5	A2				A1	A4	VSS
M	VDD	A7	A9				A11	A6	VDD
N	VSS	RESET#	A13				A14	A8	VSS

Notes: 1. A comma separates the configuration; a slash defines a selectable function. Example D7 = NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3 on page 15).

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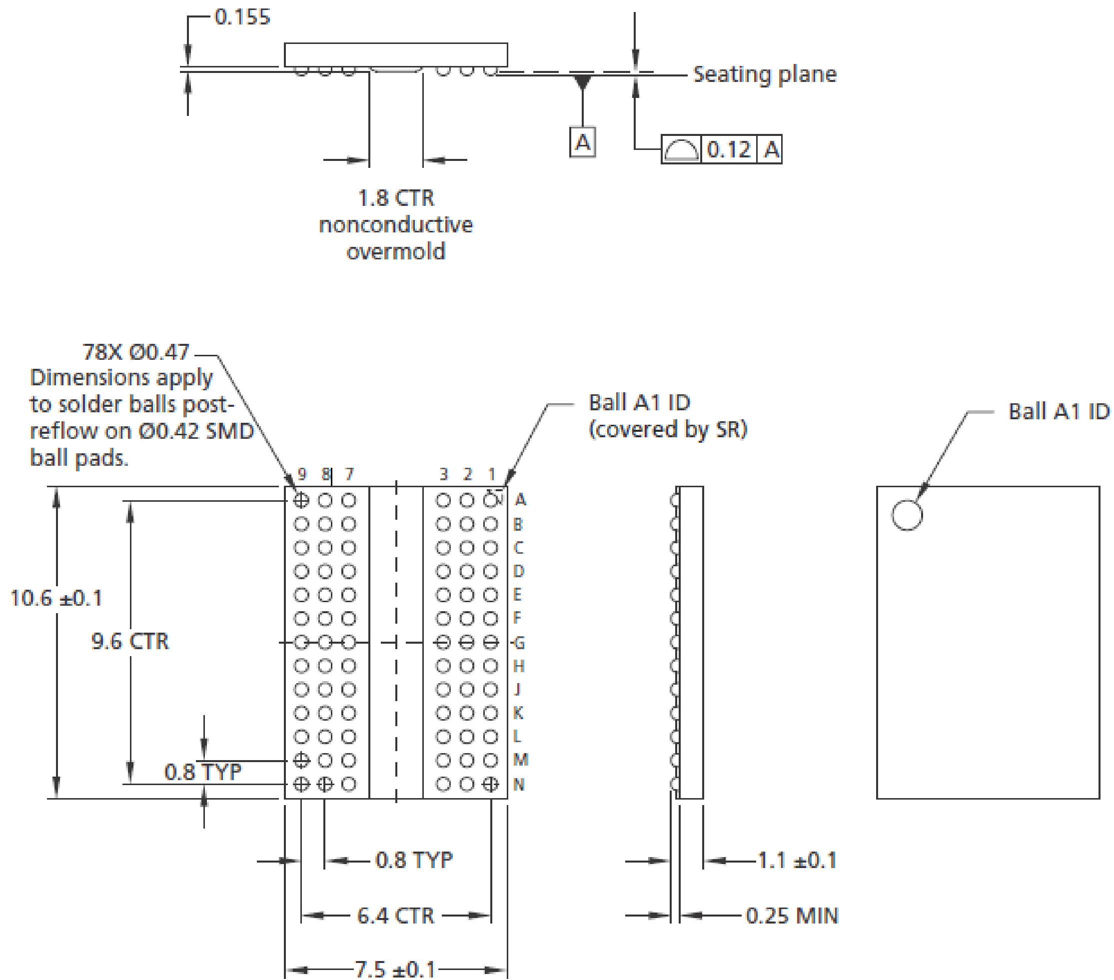
78 – Ball FBGA Package 9 X 10.6MM (GR, x8, Package)



Notes: 1. All dimensions are in millimeters.
2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu).

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