



## SDRAM DDR3 512MX8 ½ Density Device Technical Note

### Introduction

This technical note provides an overview of how the XAA512M8V90BG8RG8F-SSW0 and SSW1 DDR3 SDRAM device is configured and tested as a 2Gb device.

### Addressing

Parameter	4Gb ½ Density Device Configuration 2Gb 256M X8	4Gb Device Configuration for reference only 4Gb 512M X 8
Configuration	32MEG X 8 X 8 Banks	64MEG X 8 X 8 Banks
Refresh count	8K	8K
Row addressing	64K A0-A15	64K A0-A15
SSH0 ½ Density addressing	A15=0	N/A
SSH1 ½ Density addressing	A15=1	N/A
Bank addressing	8: BA0-BA2	8: BAO-BA2
Column addressing	2K A0-A9,11	1K A0-A9,11
Page Size	1KB	1KB

For ½ Density operation address A15 must be configured as follows:  
The SSW0 and SSW1 devices are fully tested as density full good as follows.  
SSW0 address A15 must be tied to ground  
SSW1 address A15 must be tied to Vdd.

Reference the 4Gb device datasheet for actual timing and IDD parameters

## Spectek Component Part Options and Designations

### Options

Spectek Memory  
 Address A15=0 or A15=1  
 Component depth  
 Component width  
 Design ID  
 Operating voltage  
 Refresh  
 Component package type:  
 Material type  
 Device speed

### Designation

XAA Generic Component sales  
 256MEG  
 x8  
 V90B (1/2 density device)  
 1.5V  
 8: 8K  
 RG: 78/117B 7.5X10.6MM  
 F: LEAD-FREE  
 SSW0 A15=0  
 SSW1 A15=1

### Pin Descriptions















































































Symbol	Type	Description
A0-A15	Input	<b>Address inputs:</b> Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to Vrefca. A12: When enable in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4)
BA0-BA2	Input	<b>Bank address inputs:</b> Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MRO, MR1, MR2 or MR3) is loaded during the LOAD MODE command. BA[2:0] are reference to Vrefca
CKx CKx#	Input	<b>Clock:</b> Differential clock inputs. All control command and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DSS#) is referenced to crossings of CK and CK#.
CKE	Input	<b>Clock enable:</b> Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
CS#	Input	<b>Chip select:</b> CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple ranks. CS# is considered part of the command code.
DM	Input	<b>Data mask (x8 devices only):</b> DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins.
ODT	Input	<b>On-die termination:</b> Enables (registered HIGH) and disables (register LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	<b>Command inputs:</b> RAS#, CAS# and WE# (along with CS#) define the command being entered.
RESET#	Input	<b>Reset:</b> RESET# is an active LOW CMOS input referenced to Vss. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH $\geq 0.8 \times V_{dd}$ and DC LOW $\leq 0.2 \times V_{dd}$ . RESET# assertion and deassertion are asynchronous.
DQ0- DQ7	I/O	<b>Data input/output:</b> Bidirectional data bus.
DQS DQS#	I/O	<b>Data strobe:</b> Differential data strobes. Output with read data: edge-aligned with read data: input with read data: input with write data: center-aligned with write data



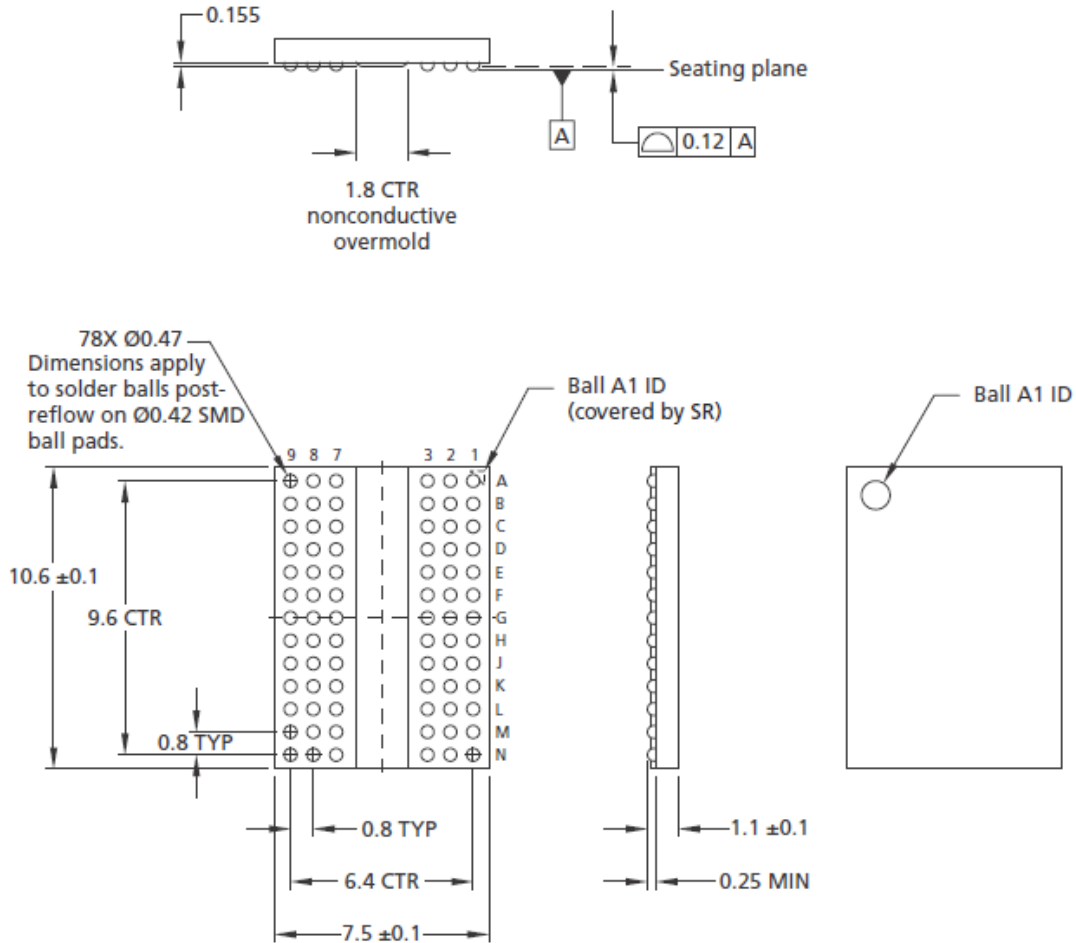
## Pin Descriptions - Continued)

Symbol	Type	Description
TDQS TDQSx#	Output	<b>Termination data strobe (x8 devices only)</b> When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance.
Vdd	Supply	<b>Power Supply:</b> 1.5V $\pm$ 0.1V.
VddQ	Supply	<b>DQ Power Supply:</b> 1.5V $\pm$ 0.1V Isolated on the device for improved noise immunity.
Vddrefca	Supply	<b>Reference voltage for control, command and address:</b> Vrefca must be maintained at all times (including self refresh) for proper device operation.
Vrefdq	Supply	<b>Reference voltage for data:</b> Vrefdq must be maintained at all times (excluding self refresh) for proper device operation.
Vss	Supply	Ground
VssQ	Supply	<b>DQ ground:</b> Isolated on the device for improved noise immunity.
ZQ	Reference	<b>External reference ball for output drive calibration:</b> This ball is tied to an external 240 ohm resistor (RZQ) which is tied to Vssq.
NC	-	<b>No connect:</b> These balls should be left unconnected (the ball has no connection to the DRAM or to other balls)
NF	-	<b>No function:</b> When configured as X4 device, these balls are NF. When configured as X8 device, these balls are defined as TDQS#,DQ[7:4].

**Ball Assignments and Descriptions**  
**78 – Ball FBGA X8 (Top View)**

	1	2	3	4	5	6	7	8	9
A	 V <sub>SS</sub>	 V <sub>DD</sub>	 NC				 NF, NF/TDQS#	 V <sub>SS</sub>	 V <sub>DD</sub>
B	 V <sub>SS</sub>	 V <sub>SSQ</sub>	 DQ0				 DM, DM/TDQS	 V <sub>SSQ</sub>	 V <sub>DDQ</sub>
C	 V <sub>DDQ</sub>	 DQ2	 DQS				 DQ1	 DQ3	 V <sub>SSQ</sub>
D	 V <sub>SSQ</sub>	 NF, DQ6	 DQS#				 V <sub>DD</sub>	 V <sub>SS</sub>	 V <sub>SSQ</sub>
E	 V <sub>REFDQ</sub>	 V <sub>DDQ</sub>	 NF, DQ4				 NF, DQ7	 NF, DQ5	 V <sub>DDQ</sub>
F	 NC	 V <sub>SS</sub>	 RAS#				 CK	 V <sub>SS</sub>	 NC
G	 ODT	 V <sub>DD</sub>	 CAS#				 CK#	 V <sub>DD</sub>	 CKE
H	 NC	 CS#	 WE#				 A10/AP	 ZQ	 NC
J	 V <sub>SS</sub>	 BA0	 BA2				 A15	 V <sub>REFCA</sub>	 V <sub>SS</sub>
K	 V <sub>DD</sub>	 A3	 A0				 A12/BC#	 BA1	 V <sub>DD</sub>
L	 V <sub>SS</sub>	 A5	 A2				 A1	 A4	 V <sub>SS</sub>
M	 V <sub>DD</sub>	 A7	 A9				 A11	 A6	 V <sub>DD</sub>
N	 V <sub>SS</sub>	 RESET#	 A13				 A14	 A8	 V <sub>SS</sub>

78 – Ball FBGA Package 7.5 X 10.6MM (RG, x8, Package)



- Notes: 1. All dimensions are in millimeters.  
 2. Solder ball material: SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)